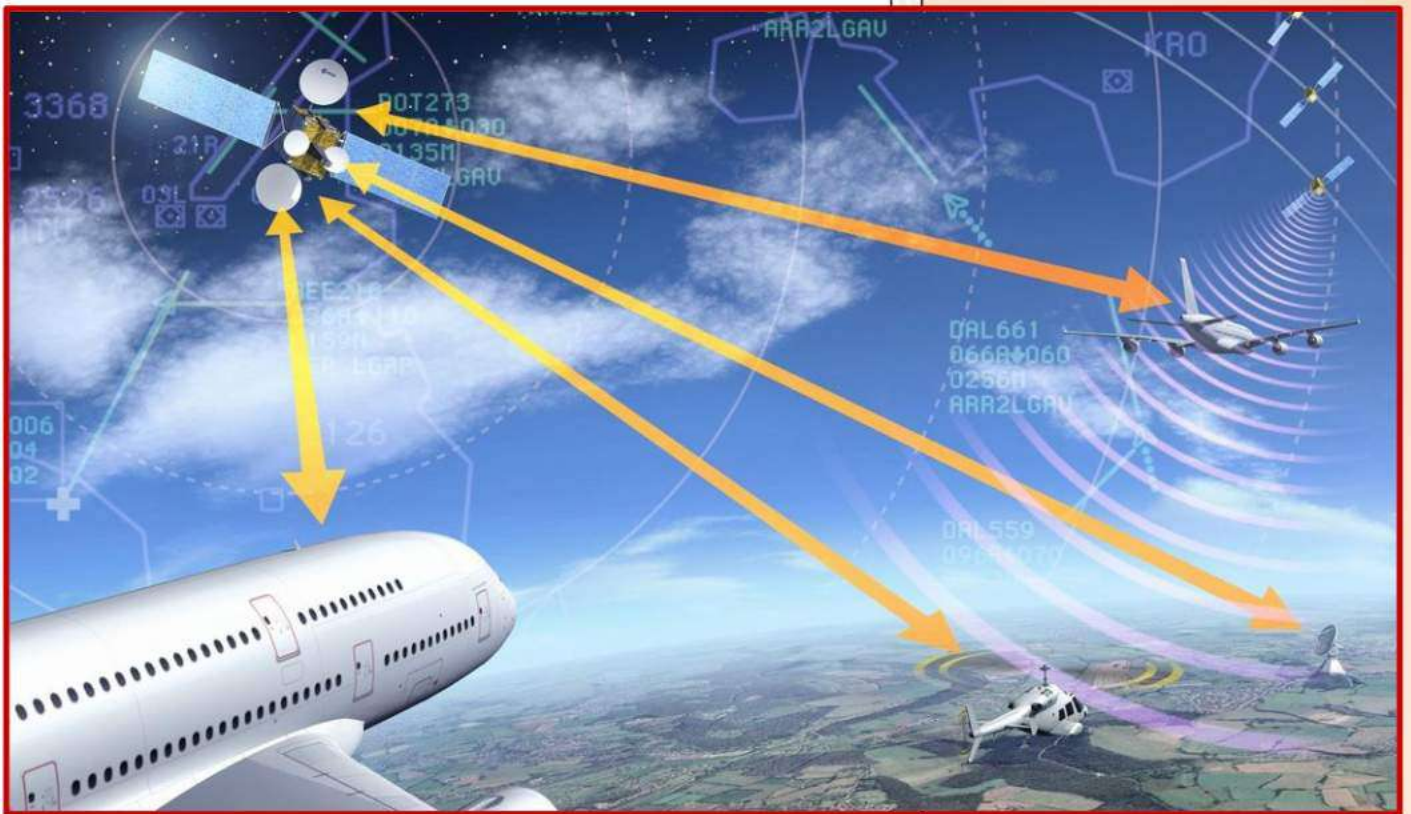# SHA-SHIB GROUP OF INSTITUTIONS
Training Notes

Module 05- Digital Techniques Electronic Instrument Systems

SHA-SHIB GROUP
EMPOWERING KNOWLEDGE THROUGH VISION

❖ The information in this book is for study/ training purposes only and no revision service will be provided to the holder.

❖ While carrying out a procedure/ work on aircraft/ aircraft equipment you must always refer to the relevant Aircraft Maintenance Manual or Equipment Manufacturer's Handbook.

❖ For health and safety in the workplace you should follow the regulations/ Guidelines as specified by the Equipment Manufacturer, your company, National Safety Authorities and National Governments.

Knowledge Levels – Category A, B1, B2, B3 and C Aircraft Maintenance Licence

Basic knowledge for categories A, B1, B2 and B3 are indicated by the allocation of knowledge levels indicators (1, 2 or 3) against each application subject. Category C applicants must meet either the category B1 or the category B2 basic knowledge levels.

The knowledge level indicators are defined as follows:

LEVEL 1

• A familiarization with the principal elements of the subject.

Objectives: The applicant should be familiar with the basic elements of the subject.

• The applicant should be able to give a simple description of the whole subject, using common words and examples.

• The applicant should be able to use typical terms.

LEVEL 2

• A general knowledge of the theoretical and practical aspects of the subject.

• An ability to apply that knowledge.

Objectives: The applicant should be able to understand the theoretical fundamentals of the subject.

• The applicant should be able to give a general description of the subject using, as appropriate, typical examples.

• The applicant should be able to use mathematical formulae in conjunction with physical laws describing the subject.

• The applicant should be able to read and understand sketches, drawings and schematics describing the subject.

• The applicant should be able to apply his knowledge in a practical manner using detailed procedures.

LEVEL 3

• A detailed knowledge of the theoretical and practical aspects of the subject.

• A capacity to combine and apply the separate elements of knowledge in a logical and comprehensive manner.

Objectives: The applicant should know the theory of the subject and interrelationships with other subjects.

• The applicant should be able to give a detailed description of the subject using theoretical fundamentals and specific examples.

• The applicant should understand and be able to use mathematical formulae related to the subject.

• The applicant should be able to read, understand and prepare sketches, simple drawings and schematics describing the subject.

• The applicant should be able to apply his knowledge in a practical manner using manufacturer's instructions.

• The applicant should be able to interpret results from various sources and measurements and apply corrective action where appropriate.

CAR – 66 ISSUE II R 2

(LICENSING OF AIRCRAFT MAINTENANCE ENGINEERS)

DIRECTORATE GENERAL OF CIVIL AVIATION

TECHNICAL CENTRE, OPP SAFDURJUNG AIRPORT, NEW DELHI

Modules	Subject	A or B1 Aero plane with		A or B1 Helicopter with		B2
		Turbine Engine (s)	Piston Engine (s)	Turbine Engine (s)	Piston Engine (s)	Avionics
1	Not Applicable					
2	Not Applicable					
3	ELECTRICAL FUNDAMENTALS	X	X	X	X	X
4	ELECTRONIC FUNDAMENTALS	X	X	X	X	X
5	DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS	X	X	X	X	X
6	MATERIALS AND HARDWARE	X	X	X	X	X
7A	MAINTENANCE PRACTICES	X	X	X	X	X
7B	MAINTENANCE PRACTICES					
8	BASIC AERODYNAMICS	X	X	X	X	X
9A	HUMAN FACTORS	X	X	X	X	X
9B	HUMAN FACTORS					
10	AVIATION LEGISLATION	X	X	X	X	X
11A	TURBINE AEROPLANE AERODYNAMICS, STRUCTURES AND SYSTEMS	X				
11B	PISTON AEROPLANE AERODYNAMICS, STRUCTURES AND SYSTEMS		X			
11C	PISTON AEROPLANE AERODYNAMICS, STRUCTURES AND SYSTEMS					
12	HELICOPTER AERODYNAMICS, STRUCTURES AND SYSTEMS			X	X	
13	AIRCRAFT AERODYNAMICS, STRUCTURES AND SYSTEMS					X
14	PROPULSION					X
15	GAS TURBINE ENGINE	X		X		
16	PISTON ENGINE		X		X	
17A	PROPELLER	X	X			
17B	PROPELLER					

SUBJECT NAME: DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

UNIT NO.	OBJECTIVE	LEVEL	
		B1	B2
5.1	**5.1 Electronic Instrument Systems** Typical systems arrangements and cockpit layout of electronic instrument systems.	2	2
5.2	**5.2 Numbering Systems** Numbering systems: binary, octal and hexadecimal; Demonstration of conversions between the decimal and binary, octal and hexadecimal systems and vice versa.	2	2
5.3	**5.3 Data Conversion** Analogue Data, Digital Data; Operation and application of analogue to digital, and digital to analogue converters, inputs and outputs, limitations of various types.	1	1
5.4	**5.4 Data Buses** Operation of data buses in aircraft systems, including knowledge of ARINC and other specifications.	2	2
5.5	**5.5 Logic Circuits** (a) Identification of common logic gate symbols, tables and equivalent circuits; Applications used for aircraft systems, schematic diagrams. (b)Interpretation of logic diagrams.	1	1
5.6	**5.6 Basic Computer Structure** (a) Computer terminology (including bit, byte, software, hardware, CPU, IC, and various memory devices such as RAM, ROM, PROM); Computer technology (as applied in aircraft systems). (b) Computer related terminology; Operation, layout and interface of the major components in a micro computer including their associated bus systems; Information contained in single and multi address instruction words;Memory associated terms; Operation of typical memory devices; Operation, advantages and disadvantages of the various data storage systems.	1	1
5.7	**5.7 Microprocessors** Functions performed and overall operation of a microprocessor; Basic operation of each of the following microprocessor elements: control and processing unit, clock, register, arithmetic logic unit.	2	2
5.8	**5.8 Integrated Circuits** Operation and use of encoders and decoders Function of encoder types Uses of medium, large and very large scale integration.	2	2
5.9	**5.9 Multiplexing** Operation, application and identification in logic diagrams of multiplexers and demultiplexers.	2	2

5.10	**5.10 Fibre Optics** Advantages and disadvantages of fibre optic data transmission over electrical wire propagation; Fibre optic data bus; Fibre optic related terms; Terminations; Couplers, control terminals, remote terminals; Application of fibre optics in aircraft systems.		
5.11	**5.11 Electronic Displays** Principles of operation of common types of displays used in modern aircraft, including Cathode Ray Tubes, Light Emitting Diodes and Liquid Crystal Display.		
5.12	**5.11 Electronic Displays** Principles of operation of common types of displays used in modern aircraft, including Cathode Ray Tubes, Light Emitting Diodes and Liquid Crystal Display.		
5.13	**5.13 Software Management Control** Awareness of restrictions, airworthiness requirements and possible catastrophic effects of unapproved changes to software programmes.		
5.14	**5.14 Electromagnetic Environment** Influence of the following phenomena on maintenance practices for electronic system: EMC-Electromagnetic Compatibility EMI-Electromagnetic Interference HIRF-High Intensity Radiated Field Lightning/lightning protection		
5.15	**5.15 Typical Electronic/Digital Aircraft Systems** General arrangement of typical electronic/digital aircraft systems and associated BITE(Built In Test Equipment) testing such as: (a) For B1 and B2 only: ACARS-ARINC Communication and Addressing and Reporting System EICAS-Engine Indication and Crew Alerting System FBW-Fly by Wire FMS-Flight Management System IRS-Inertial reference system (b) For B1, B2 and B3: ECAM-Electronic Centralised Aircraft Monitoring EFIS-Electronic Flight Instrument System GPS-Global Positioning System TCAS-Traffic Collission Avoidance system Integrated modular Avionica Cabin System , Information system		

Module 05: Enabling Objectives and Certification Statement

REVISION LOG

Sr. No.	Issue / Revision No.	Issue / Revision Date	Pages Revised	Signature

TABLE OF CONTENTS

5.1 ELECTRONICS INSTRUMENT SYSTEMS

Typical systems arrangements and cockpit layout of electronic instrument systems.

FLIGHT INSTRUMENTS

Flight instruments of paramount importance in any aircraft is the system (or systems) used for sensing and indicating the aircraft's attitude, heading, altitude and speed. In early aircraft, these instruments were simple electro- mechanical devices. Indeed, when flying under visual flight rules (VFR) rather than instrument flight rules (IFR) the pilot's most important source of information about what the aircraft was doing would have been the view out of the cockpit window! Nowadays, sophisticated avionic and display technology, augmented by digital logic and computer systems, has made it possible for an aircraft to be flown (with a few possible exceptions). Various instruments are used to provide the pilot with flight-related information, such as the aircraft's current heading, airspeed and attitude.

Modern aircraft use electronic transducers and electronic displays and indicators. Cathode ray tubes (CRT) and liquid crystal displays (LCD) are increasingly used to display this information in what has become known as a 'glass cockpit'. Modern passenger aircraft generally have a number of such displays, including those used for primary flight data and multi- function displays that can be configured to display a variety of information. We shall begin this section with a brief review of the basic flight instruments.

Basic flight instruments Crucial among the flight instruments fitted to any aircraft are those that indicate the position and attitude of the aircraft. These basic flight instruments are required to display information concerning:

* heading
* altitude
* airspeed
* rate of turn
* rate of climb (or descent)
* attitude (relative to the horizon).

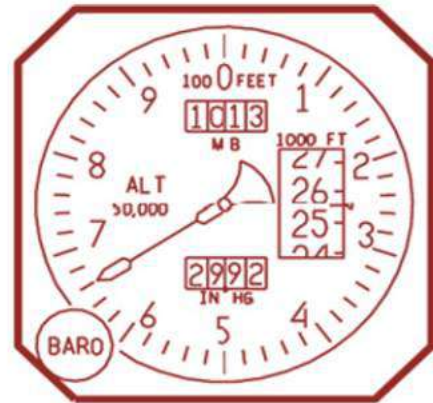The typical instrument displays shown in Figures 1.2–1.8.

Fig. 1.1 Boeing 757 Flight Instrument &
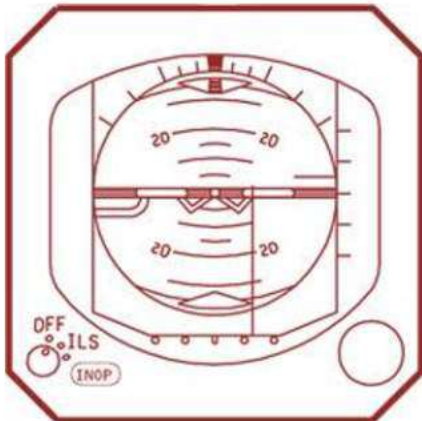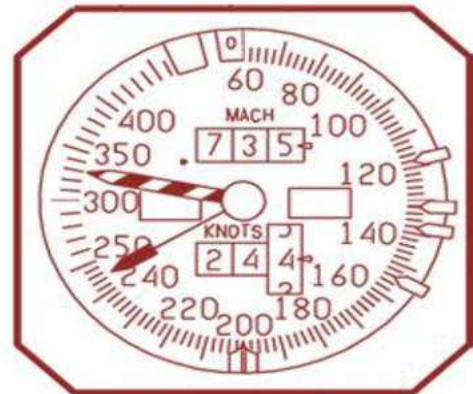
Displays
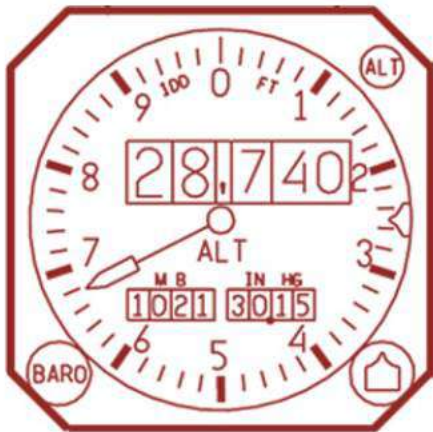
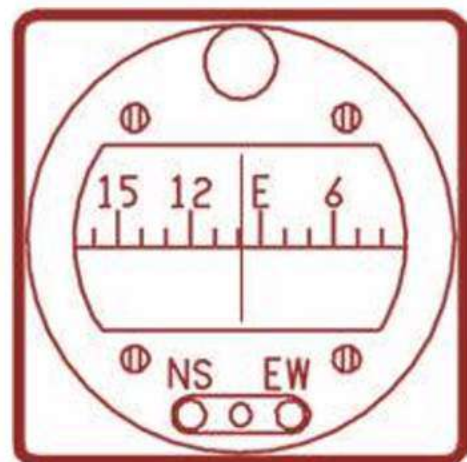1.2 Altimeter

1.3 Standby Altimeter

1.4 Attitude indicator

1.5 Airspeed indicator

1.6 Standby Airspeed indicator

1.7 Standby magnetic compass

1.8 Standby vertical speed indicator


1.9 Typical Airspeed indicator

COCKPIT LAYOUTS

Major developments in display technology and the introduction of increasingly sophisticated aircraft computer systems have meant that cockpit layouts have been subject to continuous change over the past few decades. At the same time, aircraft designers have had to respond to the need to ensure that the flight crew are not over burdened with information and that relevant data is presented in an appropriate form and at the time it is needed.

Figure 1.10 shows how the modern EFIS layouts have evolved progressively from the basic 'T' instrument configuration found in non-EFIS aircraft. Maintaining the relative position of the instruments has been important in allowing pilots to adapt from one aircraft type to another. At the same time, the large size of modern CRT and LCD displays, coupled with the ability of these instruments to display combined data (for example, heading, airspeed and altitude) has led to a less-cluttered instrument panel (see Figures
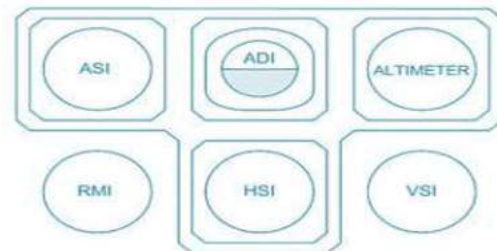
(a) Basic 'T' flight instrument configuration
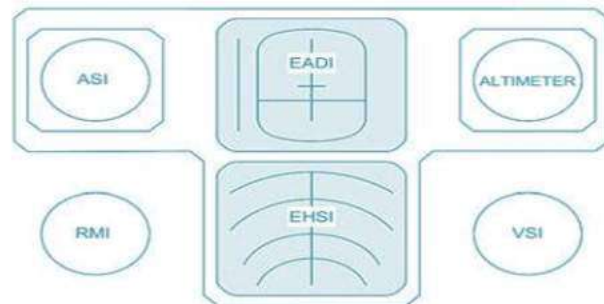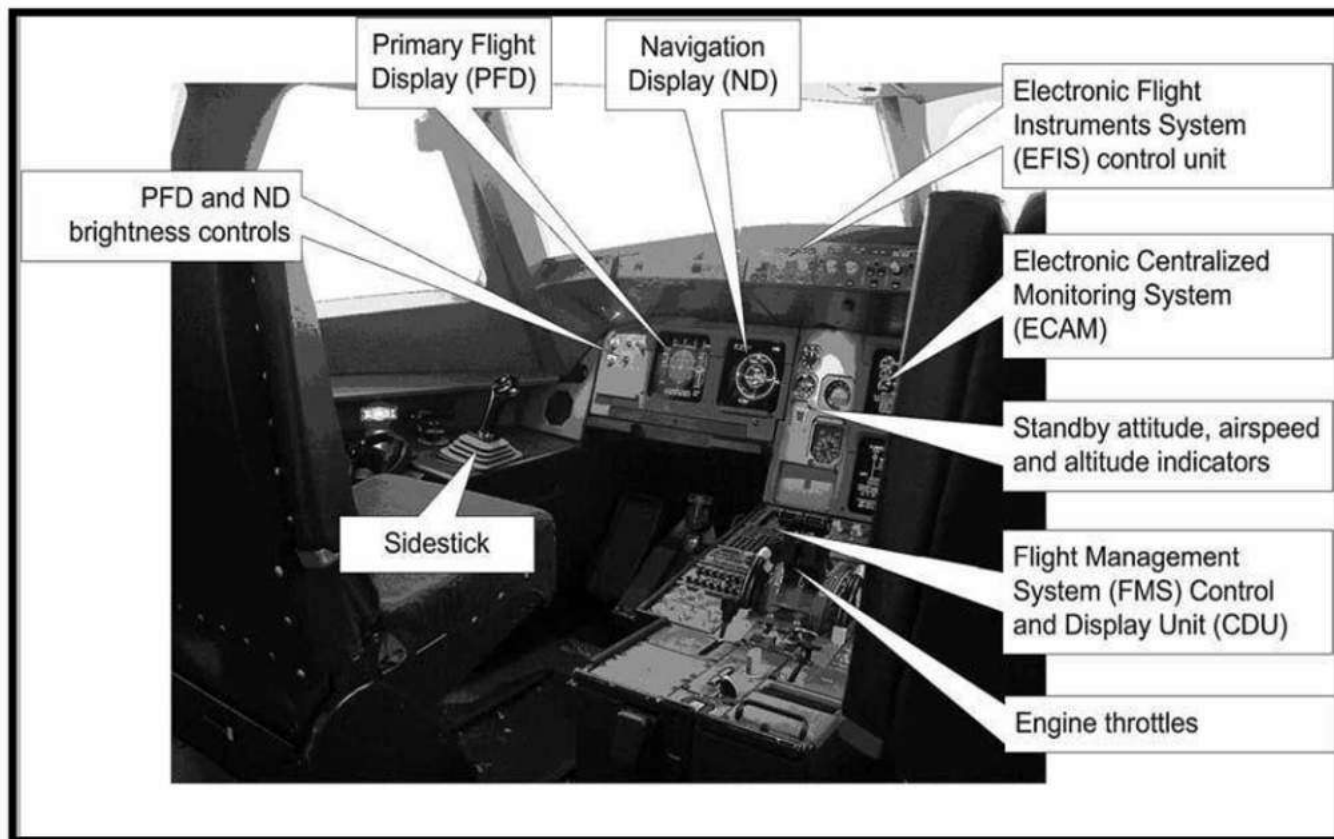

(b) Basic EFIS flight instrument configuration
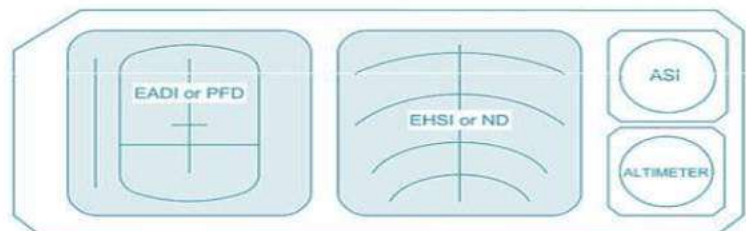
(c) Enhanced EFIS flight instrument configuration

5

1.241.26). Lastly, a number of stand by   1.10   Evolution of EFIS System
(or secondary) instruments are made available in order to provide the flight crew with reference
information which may become invaluable in the case of a malfunction in the computer system.

1.11   Captain's Flight Instruments & Display Layout onA320

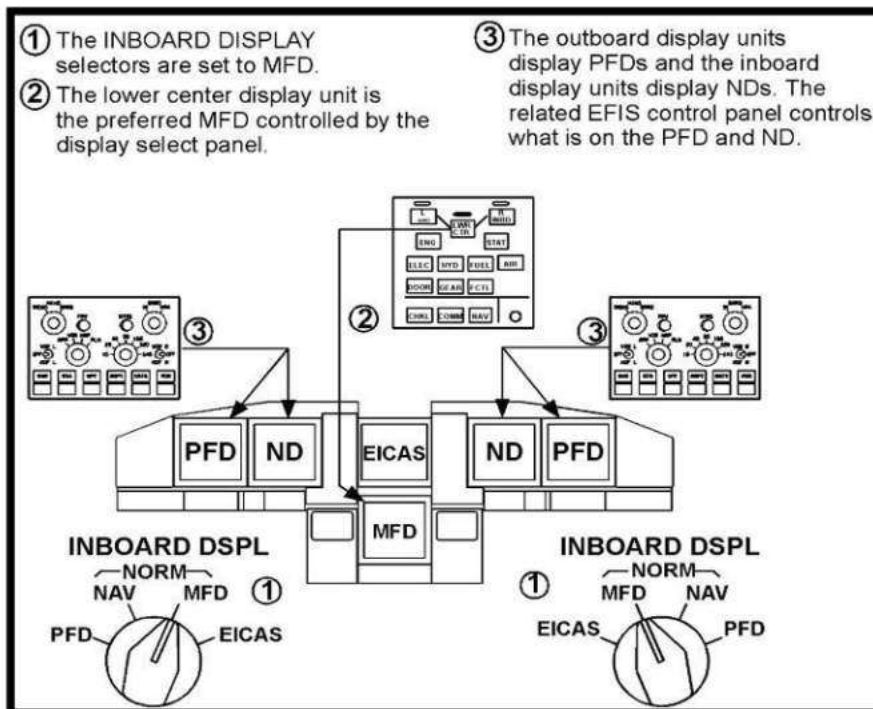1.12   Upgraded Flight Instrument on an Aero Commander690A

ELECTRONICS FLIGHT INSTRUMENT SYSTEM (EFIS)

Most of the Passenger aircraft use Electronic Flight Instrument System (EFIS) displays that has become known as the 'glass Cockpit. EFIS provides large, clear, high-resolution displays which are easy to view under wide variations of ambient light intensity. Displays can be independently selected and configured as required by the captain and first officer and the ability to display information from various data sources in a single display makes it possible for the crew to rapidly assimilate the information that they need. A notable disadvantage of EFIS is a significant increase in EMI. The two most commonly featured EFIS instruments are the Electronic Horizontal Situation Indicator (EHSI) and the Electronic Attitude Direction Indicator (EADI).
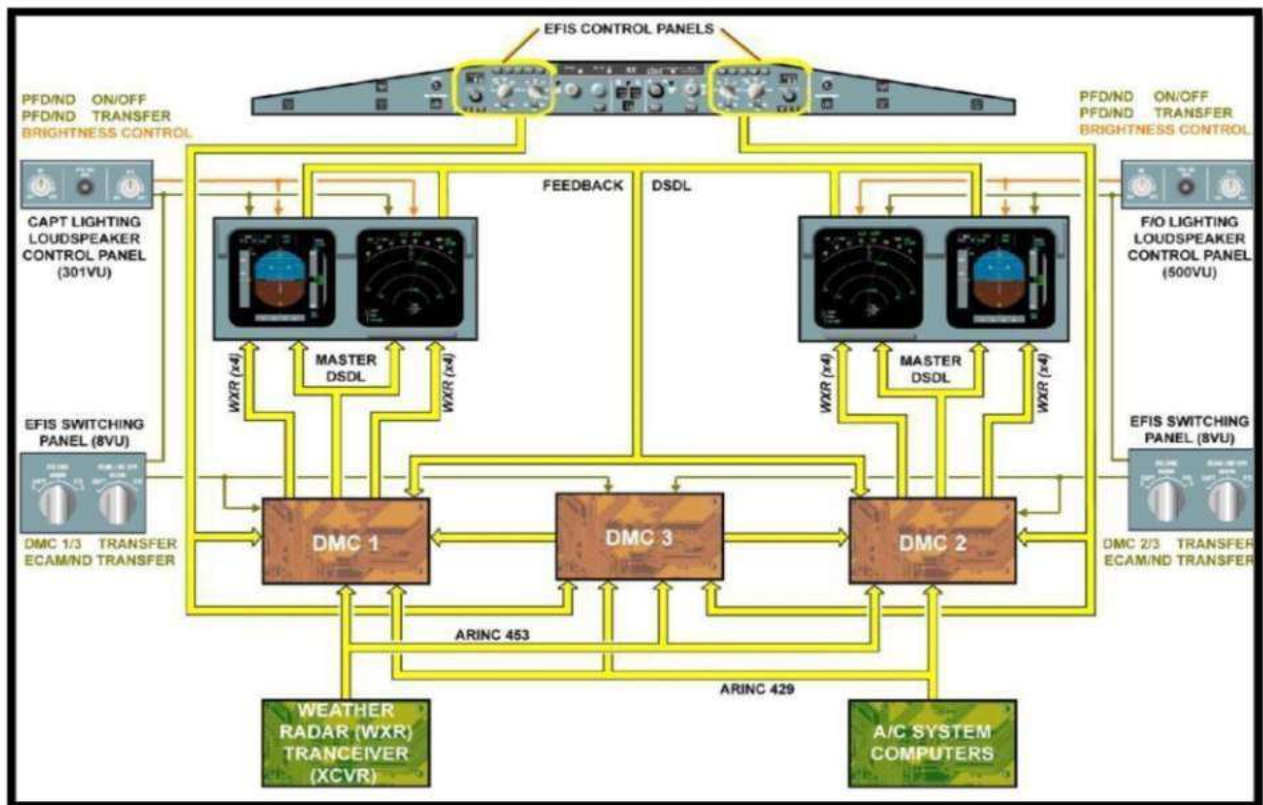
The EFIS uses input data from several sources including
- VOR/ILS/MLS
- TACAN (see later)
- Pitch, roll, heading rate and acceleration data from anAttitude Heading System Reference (AHRS) or conventional vertical gyro
- Compass system
- Radar altimeter
- Air data system
- Distance Measuring Equipment (DME)
- Area Navigation System (RNAV)
- Vertical Navigation System (VNAV)
- Weather Radar System (WXR)
- Automatic Finder (ADF)

Typical EFIS displays are shown in fig 1.13 & 1.14.

① The INBOARD DISPLAY selectors are set to MFD.
② The lower center display unit is the preferred MFD controlled by the display select panel.
③ The outboard display units display PFDs and the inboard display units display NDs. The related EFIS control panel controls what is on the PFD and ND.

1.13   Typical EFIS Display forBoeing

1.14   Typical EFIS for Airbus

PRIMARY FLIGHT DISPLAY (PFD)

The PFDs present a dynamic color display of all the parameters necessary for flight path control. The PFDs provide the following Information:

- Flight Mode Annunciation
- Airspeed
- Altitude
- Vertical Speed
- Attitude
- Steering Information
- Radio Altitude
- Instrument Landing System Display
- Approach Minimums
- Heading/ Track Indications
- Time Critical Warnings

Failure flags are displayed for airplane system failures. Displayed information is removed or replaced by dashes if no valid information is available to the display system (because of out-of range or malfunctioning navigation aids). Displays are removed when a source fails or when no system source information is available.

Expanded mode with a partial compass rose and a centered mode with a full compass rose.

ND Modes / MAP Mode

The MAP mode is recommended for most phases of flight. Presented track up, this mode shows airplane position relative to the route of flight against a moving map background.
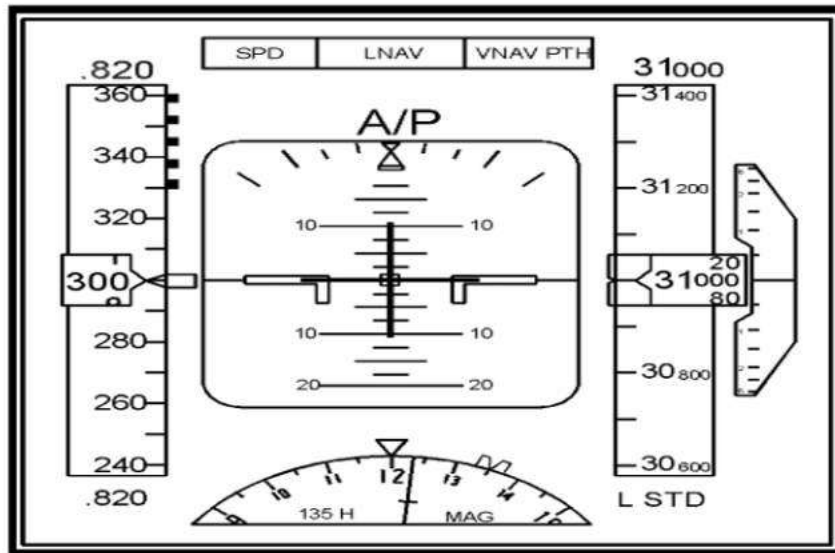
1.15 Typical PFD display NAVIGATION DISPLAY (ND)

The NDs provide a mode-selectable color flight progress display. The modes are:
The MAP, VOR, and APP modes can be switched between an

VOR AND APPROACH MODES
The VOR and APP modes are presented heading up. The VOR and APP modes display track, heading, and wind speed and direction with VOR navigation or ILS approach information.

PLAN MODE
The PLN mode is presented true north up. The active route may be viewed using the STEP prompt on the CDU LEGS pages.

ND INFORMATION

HEADING
Heading is supplied by the FMC or Air Data Inertial Reference System (ADIRS). The ND compass rose can be referenced to magnetic north or true north. The heading reference switch is used to manually select magnetic or true reference. The compass display is automatically referenced to true north when the airplane is north of 82° north or south of 82° south latitude, or near the magnetic poles with the heading reference switch in NORM.

TRACK
Track is supplied by the FMC during normal operation and by the CDU when in alternate navigation.

TRAFFIC
Traffic information from the TCAS can be displayed on the ND

WEATHER RADAR
Weather radar information can be displayed on the ND.

FAILURE FLAGS AND MESSAGES

Failure flags are displayed for system failures or invalid information. Indications are removed or replaced by dashes when source system information is not available. The message EXCESS DATA is displayed if the amount of information sent to the ND exceeds the display capability. When this occurs, the primary display system removes information from the center of the display outward; information near the outer selected range area is still displayed. The message can be removed by:

* Reducing the amount of map information,
* Reducing range, or
* Deselecting one or more of the EFIS control panel map switches (STA, WPT, ARPT, DATA, POS).
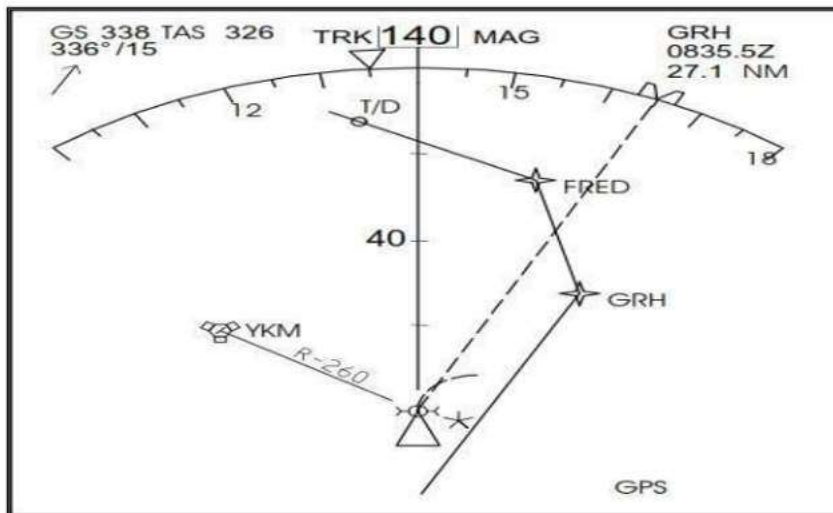
1.16   Typical ND display when POS (Position) Map Switchis Selected

ECAM (ENHANCED SYSTEM)

On the enhanced system, the only difference on this schematic is that DMC 1 supplies both ECAM displays and DMC 2 is also a backup for ECAM displays. The DMCs acquire data and transmit it to the Display Units which generate the images. Under normal circumstances, DMC 1 supplies both ECAM display & DMC 2 and 3 are available as a backup. The FWCs, heart of the ECAM system, receive data from the A/C systems to generate red warnings, the SDACs to generate amber cautions. The FWCs then supply.

* The DMCs for the display of alert messages,
* The attention getters,
* The loudspeakers with aural alerts and synthetic voice messages.
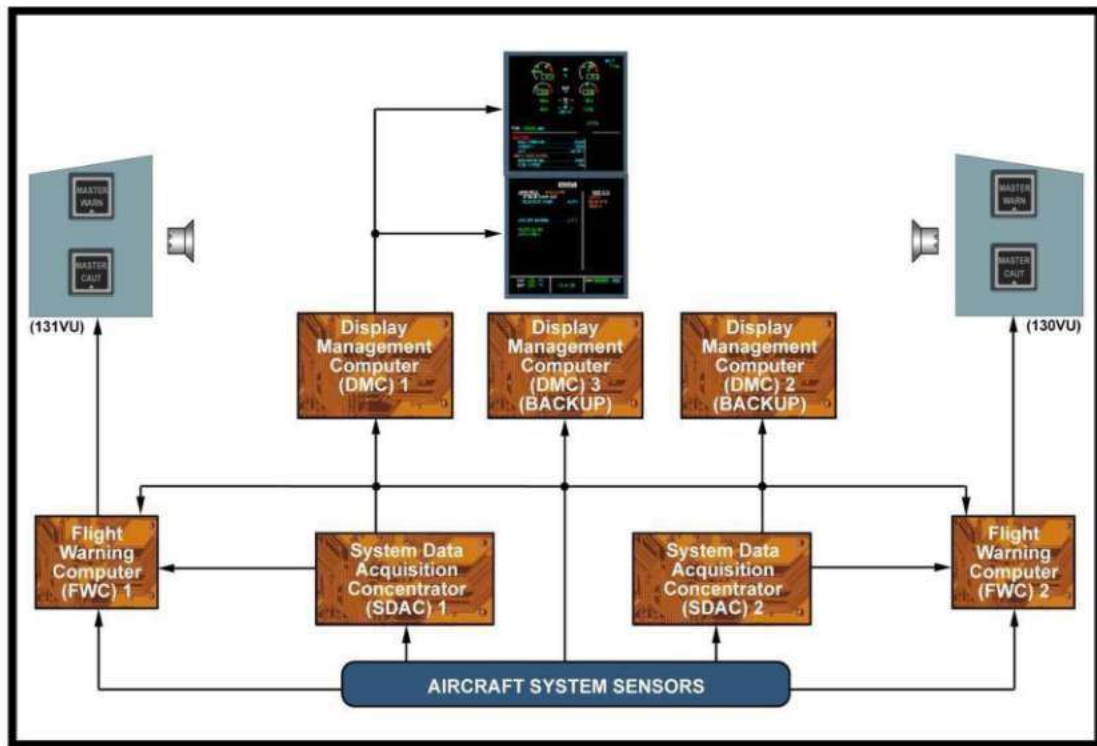
ECAM OPERATION GENERAL ARCHITECTURE

The Electronic Centralized Aircraft Monitoring (ECAM) fulfils three main Functions:

1. Data acquisition and concentration,
2. Data warning computation,
3. Warning announcement and data display.

Data acquisition is shared between, The System Data Acquisition Concentrators (SDACs), the Flight Warning Computers (FWCs) and the Display Management Computers (DMCs). Data warning computation and memo information are achieved by the FWCs. Warning announcement and data display is made through loudspeakers and Display Units (DUs).The FWCs give aural and visual

information in order to Know, in real time, all the system failures and dangerous configurations with their level of seriousness, identify the systems or circuits affected by a failure, take the appropriate corrective action


1.17   ECAM Architecture

ENGINE/WARNING DISPLAY PRESENTATION GENERAL OVERVIEW

The Engine/Warning Display (EWD) is normally on the upper Electronic Centralized Aircraft Monitoring (ECAM) Display Unit (DU). It is divided into two areas: the upper area and the lower area. (See figure 1.18)

1.   The upper area displays: Engine primary parameters, Fuel On Board (FOB), Slats and flaps position.
2.   The lower area is used for: Warning and caution messages and Memo messages.
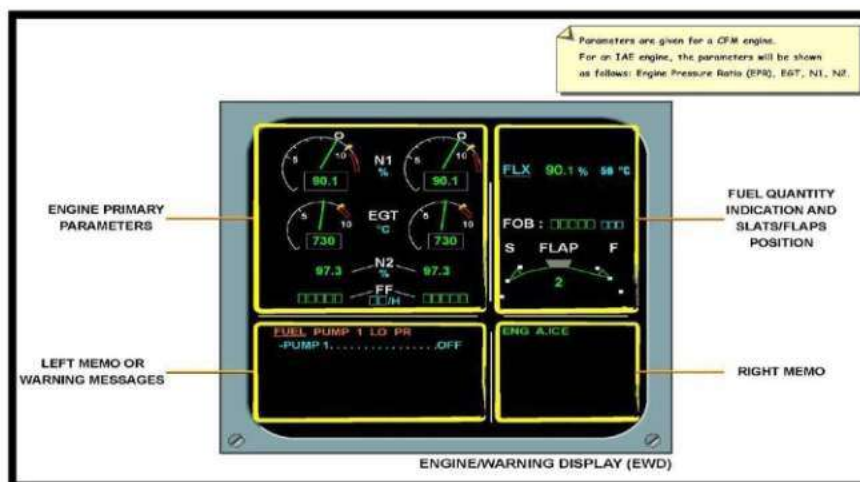
1.18   General Overview of ECAM

ENGINE/WARNING DISPLAY AREAS

1. UPPER AREA

The symbols of the upper area are permanently displayed. The parameters are provided in the form of analog and/or digital indications (refer to related chapter for detailed description).

2. LEFT MEMO AREA

Takeoff (TO) or landing memo, normal memo, independent failure messages, or primary failure messages and actions to do are displayed in the left memo area. As soon as a failure is detected, the memo messages are replaced by warning/caution messages.

3. RIGHT MEMO AREA

Normal memo and secondary failure messages are displayed in the right memo area. For example when an engine anti ice P/B is set to ON, ENG Anti ICE appears on the right memo area. During TO and landing, most of the warnings are inhibited to avoid distraction of the crew. For example, at TO, when the second engine is set to TO power and until the aircraft has reachedFigure 1.500 ft, TO INHIB is displayed.

TYPE OF FAILURES IN ECAM GENERAL

The failures may be of three different types, independently of their classification. There are 3 separate types of warnings or cautions:

1.   Those associated with an independent failure,
2.   Those associated with a primary failure,
3.   Those associated with a secondary failure.

1. INDEPENDENT FAILURE

An independent failure is a failure, which affects an isolated item of equipment or system without affecting another one. Example: Flight Warning Computer (FWC) 1 failure.

NOTE: An independent failure is displayed with the title underlined.

2. PRIMARY FAILURE

A primary failure is a failure of an item of equipment or system causing the loss of other equipment. Example: Green hydraulic system failure may lead to the loss of a pair of spoilers.

3. SECONDARY FAILURE

A secondary failure is a loss of an item of equipment or system resulting from a primary failure. Example: Loss of a pair of spoilers after a hydraulic system failure. The titles of the system pages corresponding to the secondary failures are indicated on the lower right part of the Engine/Warning Display (EWD) by an asterisk.

NOTE: This part can be used if necessary to display heading titles of warnings if the left part of the EWD is full.

ENGINE INDICATION AND CREW ALERTING SYSTEM (EICAS)

The Engine Indication and Crew Alerting System (EICAS) receive and processes signals from engine and system sensors. The architecture of the system (EICAS) starts from the engine and system sensors. In this system there are two Data Acquisition Units (DAU's) which collect data from systems of all parts of the aircraft. The DAU 1 collects the data from the sources located in the front part of the aircraft and engine # Figure 1. The DAU 2 collects the data from the sources located in the rear part of the aircraft and engine # 2. Either message or indication goes through DAU, where the analog signal is changed to a digital one, and sent to the integrated computer (IC-600). This system also uses reversion switches for display units, data acquisition unit, and symbol generators. The Data Acquisition Unit (DAU) receives analog and digital signals for using them in the EICAS. The following aircraft systems are interfacing with the EICAS for indication and alert functions:
*   Power plant
*   Landing gear
*   Flaps
*   Spoilers
*   Pressurization
*   APU
*   Trims
*   Brakes
*   Hydraulics
*   Electrical
*   Fuel
*   Ice/rain protection
*   Air conditioning
*   (Aircraft with CAT-III a configuration) Head-up guidance system.
*   Oxygen
*   Doors

The following aircraft systems are interfacing the EICAS for alerting purposes only:
*   Air turbine starter
*   Master announcement
*   Aural warning
*   Central Maintenance Computer (CMC)
*   (E) GPWS/Wind shear
*   Rudder
*   Smoke
*   Stall protection system
*   Thrust reverser

The integrated architecture of the system uses the EICAS display and MFD's for indications. The Radio Management Units, two separate displays which are normally used for Radio Management purpose, can be used to display EICAS information (engineparameters and critical messages) as a backup in case of failure of an Integrated Computer.

EICAS PRIMARY FORMAT

The EICAS primary format is always shown at the DU-3, and is divided in three parts:
- Engine Indications
- System Indications
- Crew Alerting

ENGINE INDICATION OF OTHER AIRCRAFT SYSTEMS

The most important parameters of the engines are presented on the EICAS primary format on DU 3 Figure 1.19 highlights the Indication of the other aircraft systems those are continuously shown on the EICAS primary Format. The EICAS continuously monitors the status of various aircraft and avionics system, and generates messages for the flight crew members. Each IC-600 receives warning, caution, advisory, and status signals from systems. The IC that controls the EICAS display, which is selected through the reversionary panel, will have the messages displayed. The CAS area location is at the upper right field of the EICAS display. This field has the capability of 16 lines of 18 characters per line. The last line shows the status line. More than 150 messages will be shown on the CAS according to the message type. The message types are warning, caution, and advisory. Warning (red color) messages are displayed on top, followed by caution (amber color) messages, and advisory (cyan color) messages. The newest message will be displayed on top of its respective queue. When a new message occurs, the message will flash.
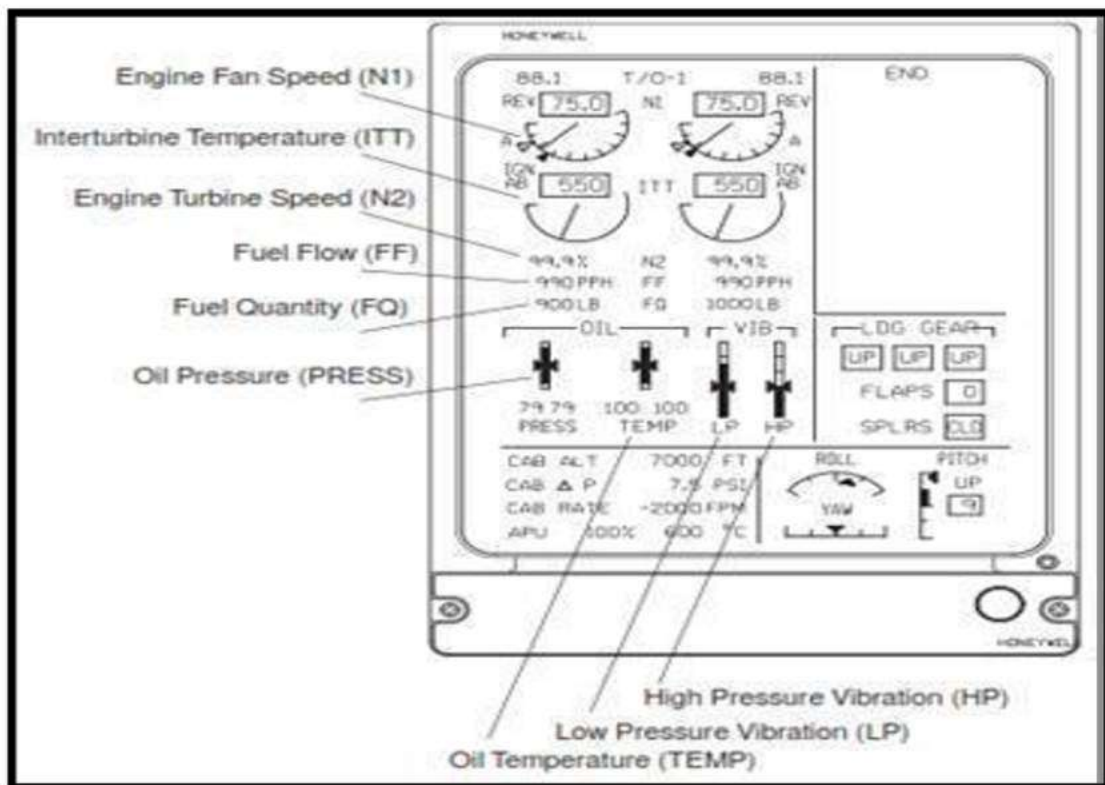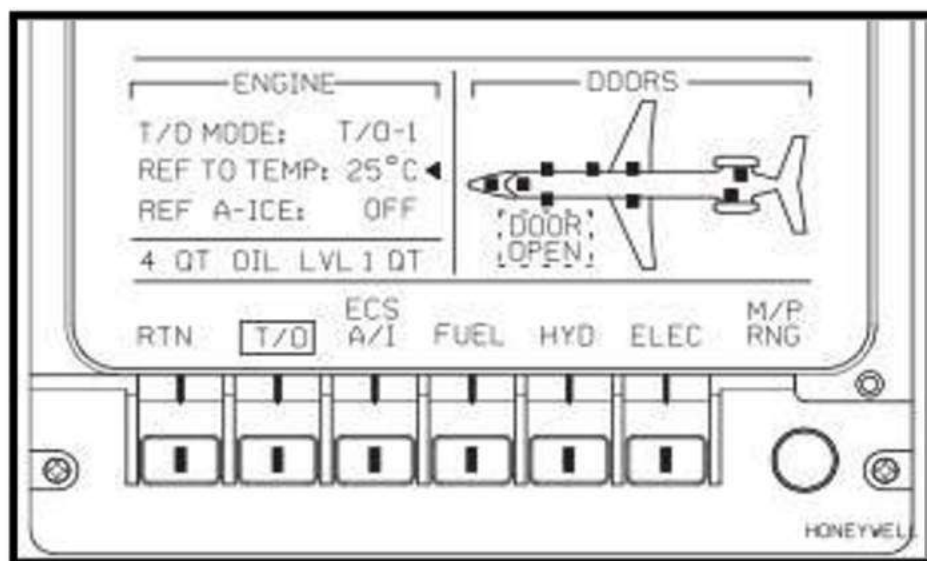

1.19   Engine indication on EICAS display
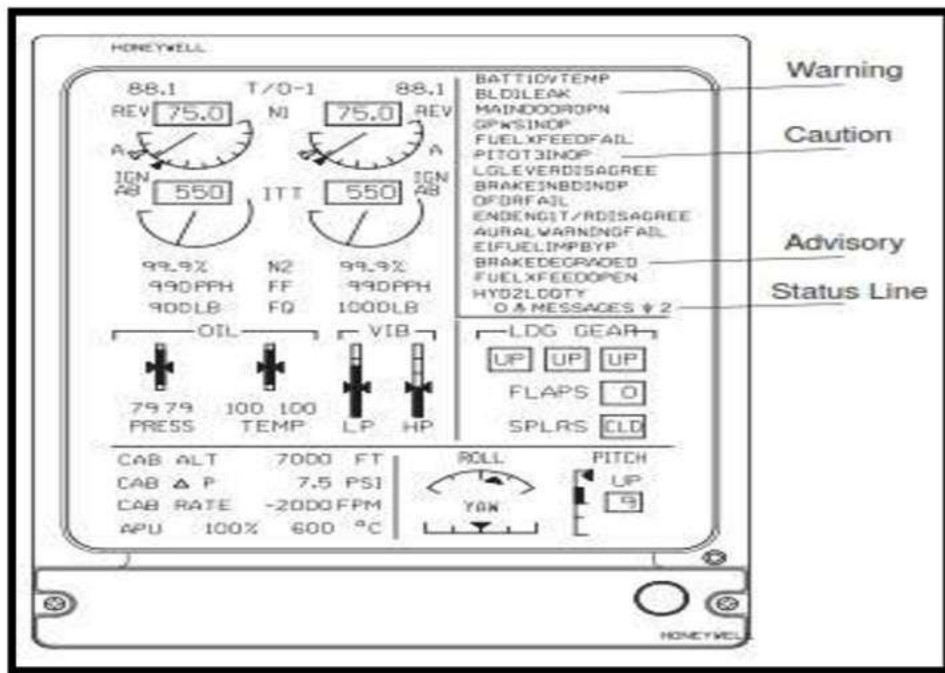
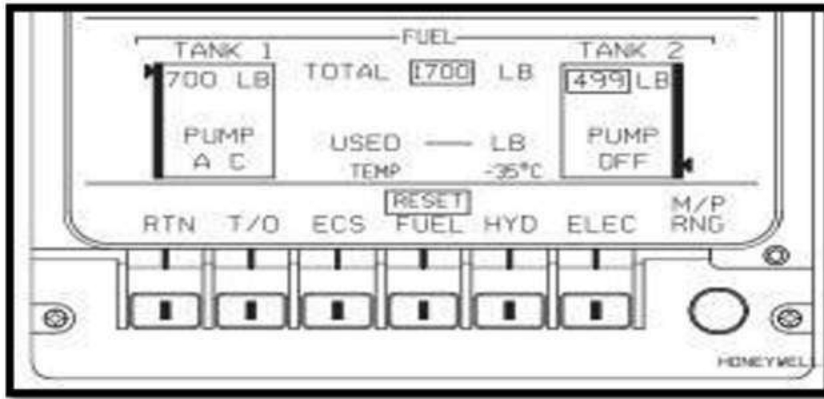1.20 Crew Alerting Messages on EICAS display.

MULTI-FUNCTION DISPLAY - MFD

The MFD (DU 2/4) is similar to DU-3, but, through its menu, you can get access to system pages, as follows:
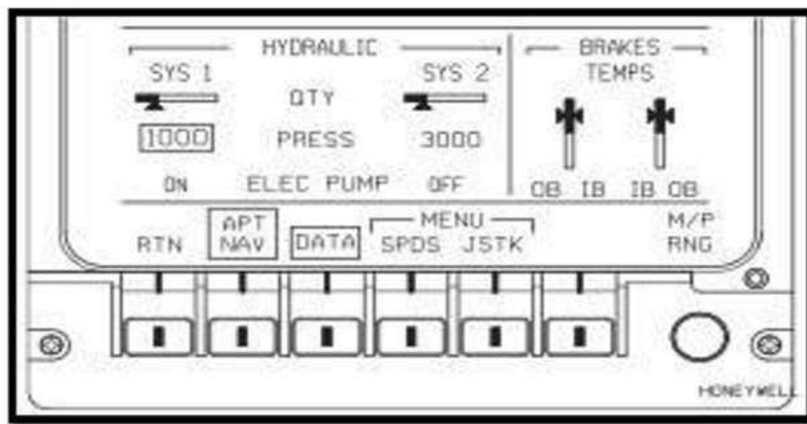
- Take-off Page
- ECS Page
- Fuel Page
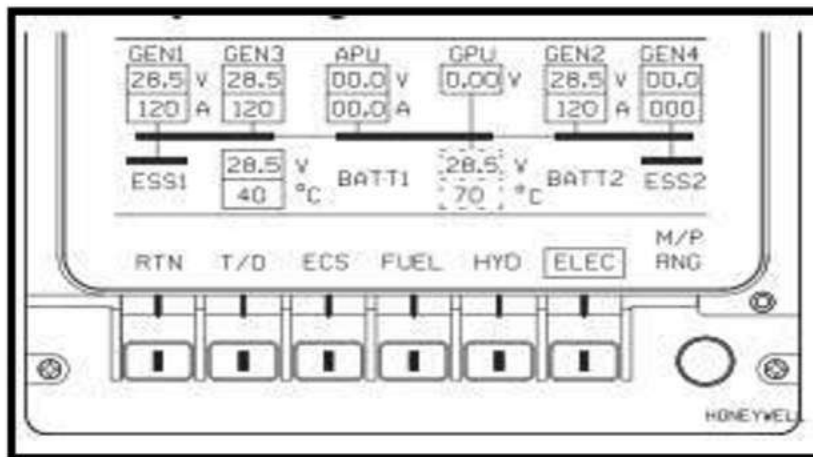- Hydraulic/ Brake Page
- Electrical Page

1.21 Take Off Page (MFD Partially Displayed)

1.22   Fuel System Page

1.23   Hydraulics System Page

1.24   Electrical System Page

5.2 NUMBERING SYSTEMS

INTRODUCTION

The signals in digital logic and computer systems are conveyed along individual electrical conductors and also using multiple wiring arrangements where several conductors are used to convey signals from one place to another in what is known as a bus system. the number of individual bus lines depends upon the particular bus standard employed however signals on the individual lines, no matter what they are used for nor how they are organised, can exist in only two basic states: logic 0 ('low' or 'off') or logic 1 ('high' or 'on'). Thus information within a digital system is represented in the form of a sequence of 1s and 0s known as binarydata.

Since binary numbers (particularly large ones) are not very convenient for human use, we often convert binary numbers to other forms of number that are easier to recognize and manipulate. These number systems include hexadecimal (base 16) and octal (base 8). This chapter is designed to introduce you to the different types of number system as well as the process of conversion from one type to another.

DECIMAL NUMBERS

The decimal numbers (Denary) that we are all very familiar with use the base 10. In this system the weight of each digit is 10 times as great as the digit immediately to its right. The right most digit of a decimal integer (i.e. a whole number) is the unit's place (10^0), the digit to its left is the ten's digit (10^1), the next is the hundred's digit (10), and so on. The valid digits in a decimal number are 0 to 9. Figures 2.1 and 2.2 show two examples of how decimal numbers are constructed
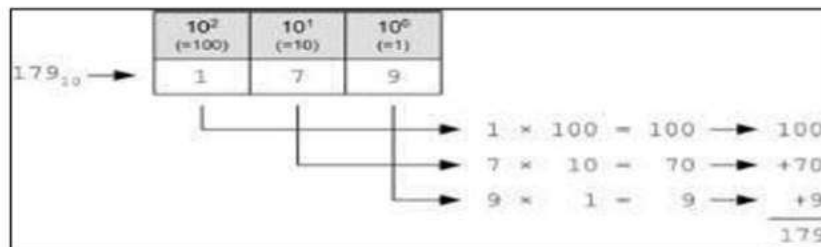

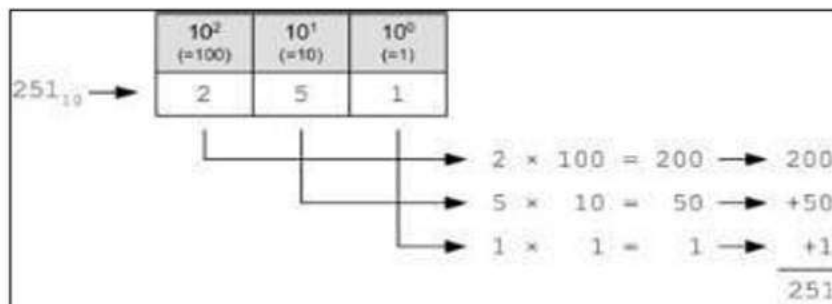Figure 2.1: An example showing how the decimal number 179 is constructed

Figure 2.2: An example showing how the decimal number 251 is constructed

Note that we have used the suffix '10' to indicate that the number is a decimal. So, 17910 and 251

are both decimal (or base 10) numbers. The use of subscripts helps us to avoid confusion about what number base we are actually dealing with.

BINARY NUMBERS

In the binary system (base 2), the weight of each digit is two times as great as the digit immediately to its right. The rightmost digit of a binary integer is the one's digit, the next digit to the left is the two's digit, next is the four's digit, then the eight's digit, and so on. The valid digits in the binary system are 0 and 1. Figure 2.3 shows an example of a binary number (note the use of the suffix '2' to indicate the number base). The binary numbers that are equivalent to the decimal numbers 0 to 9 are shown in Table 2.1. Notice how the most significant digit (MSD) is on the left and the least significant digit (LSD) appears on the right. In the table, the MSD has a weight of 2^3 (or 8 in decimal) whilst the LSD has a weight of 2^0 (or 1 in decimal). Since the MSD and LSD are represented by binary digits (either 0 or 1) we often refer to them as the most significant bit (MSB) and least significant bit (LSB) respectively, as shown in Fig.2.4.

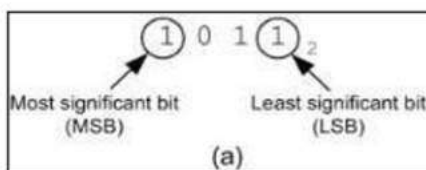|	2^3 (=8)	2^2 (=4)	2^1 (=2)	2^0 (=1)
$1011_2 \rightarrow$	1	0	1	1

Figure 2.3 : Example of a Binary Number

Figure 2.4: MSB and LSB in Binary Numbers

BINARY TO DECIMAL CONVERSION

In order to convert a binary number to its equivalent decimal number we can determine the value of each successive binary digit, multiply it by the column value (in terms of the power of the base) and then simply add the values up. For example, to convert the binary number 1011, we take each digit and multiply it by the binary weight of the digit position (8, 4, 2 and 1) and add the result, as shown in Fig. 2.5below.

Figure 2.5: Example of Binary to Decimal Conversion DECIMAL TO BINARY CONVERSION

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There are two basic methods for converting decimal numbers to their equivalent in binary. The first method involves breaking the number down into a succession of numbers that are each powers of 2 and then placing the relevant digit (either a 0 or a 1) in the respective digit position, as shown in Fig. 2.6. Another method involves successive division by two, retaining the remainder as a binary digit and then using the result as the next number to be divided, as shown in Figure 2.7.
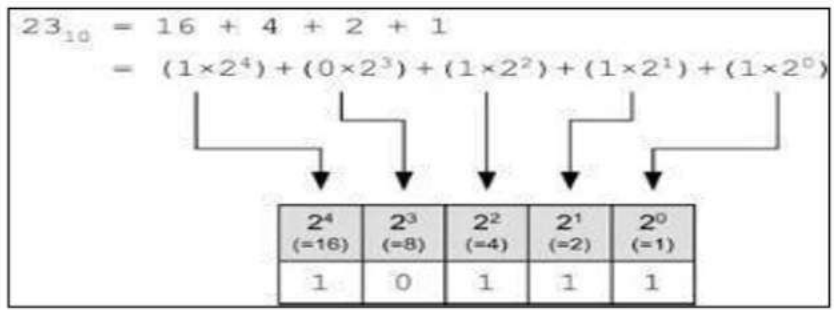

Figure 2.6: Example of Decimal to Binary Conversion

BINARY CODED DECIMAL

The system of binary numbers that we have looked at so far is more correctly known as natural binary. Another form of binary number commonly used in digital logic circuits is known as binary coded decimal (BCD). In this simpler system, binary conversion to and from decimal numbers involves arranging binary numbers in groups of four binary digits from right to left, each of which corresponds to a single decimal digit, as shown in Figures 2.8 and 2
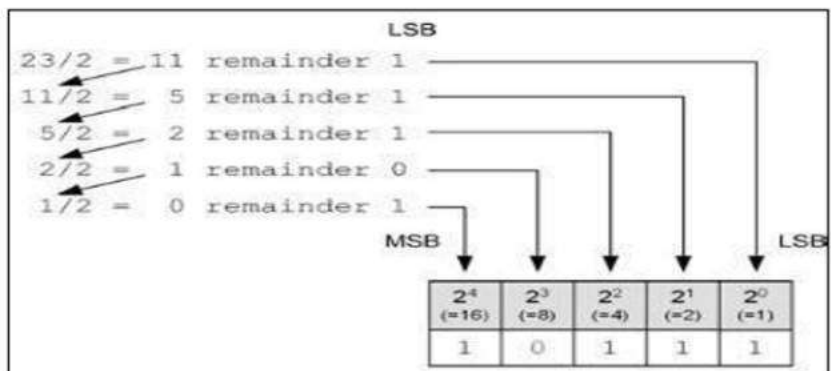

Figure 2.7: Example of Decimal to Binary Conversion using Successive Division
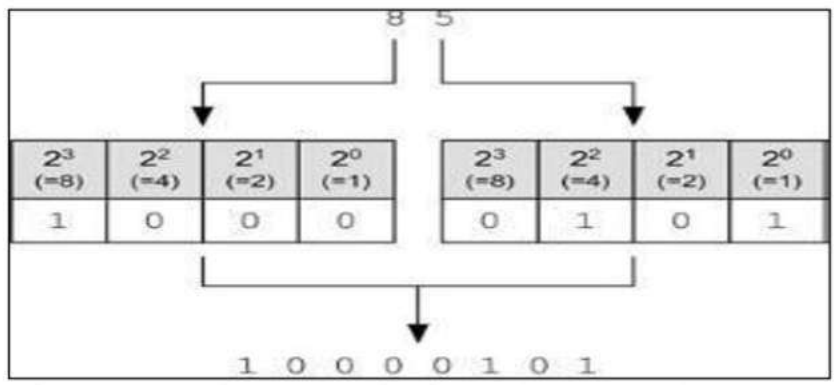

Figure 2.8 : Example of Converting the Decimal Number 85 to Binary Coded Decimal (BCD)
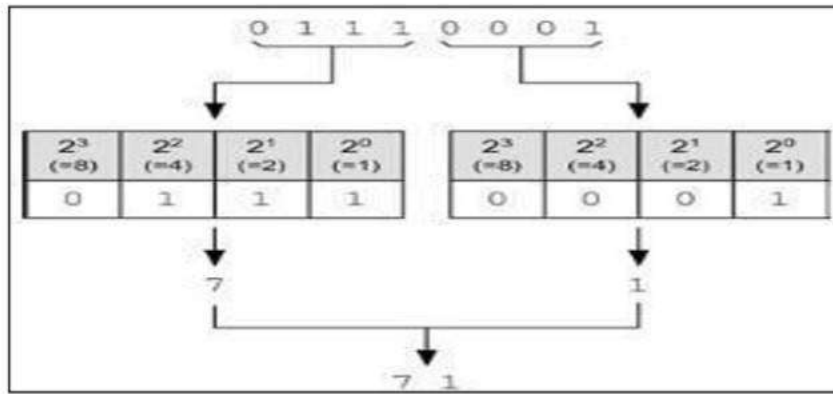
Figure 2.9: Example of Converting the BCD number 01110001to Decimal

ONE'S COMPLEMENT

The one's complement of a binary number is formed by inverting the value of each digit of the original binary number (i.e. replacing 1s with 0s and 0s with 1s) So, for example, the one's complement of the binary number 1010 is simply 0101. Similarly, the one's complement of 01110001 is 10001110. Note that if you add the one's complement of a number to the original number the result will be all 1s, as shown in Figure2.10.

Fig: 2.10

TWO'S COMPLEMENT

Two's complement notation is frequently used to represent negative numbers in computer mathematics (with only one possible code for zero—unlike one's complement notation). The two's complement of a binary number is formed by inverting the digits of the original binary number and then adding 1 to the result. So, for example, the two's complement of the binary number 1001 is 0111. Similarly, the two's complement of 01110001 is 10001111. When two's complement notation is used to represent negative numbers the most significant digit (MSD) is always a 1. Figure 2.11 shows two examples of finding the two's complement of a binary number. In the case of Figure 2.11(b) it is

Figure 2.11 : Method of finding the Two's Complement of a Binary Number

OCTAL NUMBERS

The octal number system is used as a more compact way of representing binary numbers. Because octal consists of eight digits (0 to 7), a single octal digit can replace three binary digits. Putting this another way, by arranging a binary number into groups of three binary digits (or bits) we can replace each group by a single octal digit, see Figure 2.12, the weight of each digit in an octal number is eight times as great as the digit immediately to its right. The rightmost digit of an octal number is the unit's place (8^0), the digit to its left is the eight's digit (8^1), the next is the 64's digit (8^2), and soon.

OCTAL TO DECIMAL CONVERSION

In order to convert a binary number to a decimal number we can determine the value of each successive octal digit, multiply it by the column value (in terms of the power of the base) and simply add the values up. For example, the octal number 207 is converted by taking each digit and then multiplying it by the octal weight of the digit position and adding the result, as shown in Figure2.13.
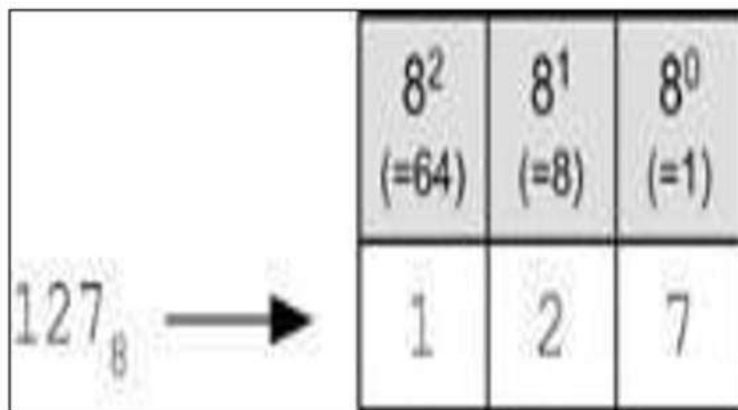

Figure 2.12: Example of an Octal Number
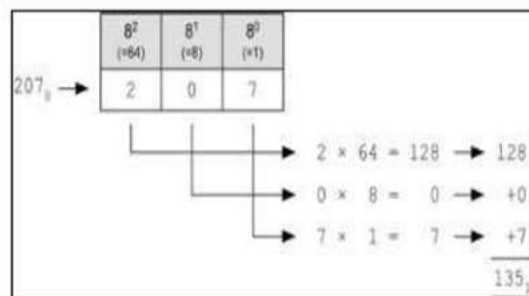
Figure 2.13 Example of an Octal Number to decimal number

DECIMAL TO OCTAL CONVERSION

As with decimal to binary conversion, there are two methods for converting decimal numbers to octal. The first method involves breaking the number down into a succession of numbers that are each powers of 8 and then placing the relevant digit (having a value between 0 and 7) in the respective digit position, as shown in Figure2.14.
The other method of decimal to octal conversion involves successive division by eight, retaining the remainder as a digit (with a value between 0 and 7) before using the result as the next number to be

divided, as shown in Figure 2.15. Note how the octal number is built up in reverse order i.e. with the last remainder as the MSD and the first remainder as the LSD

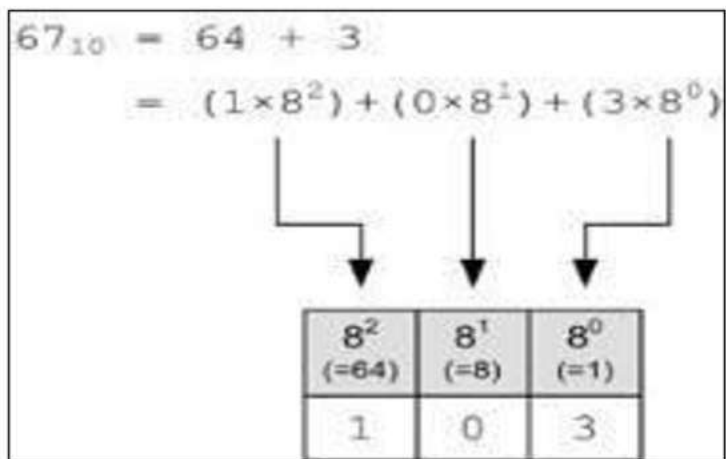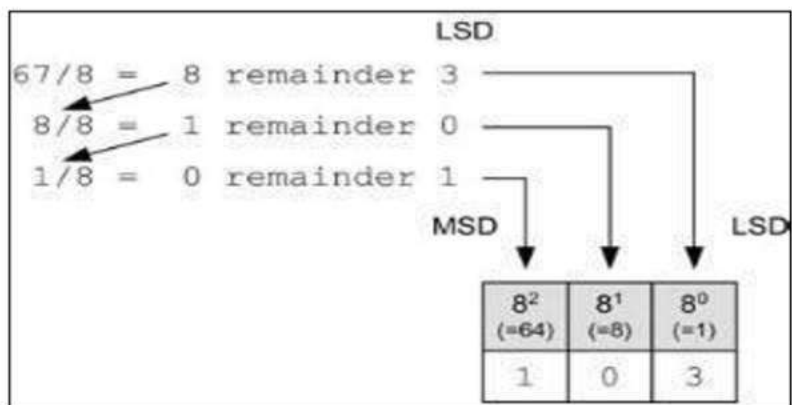Figure 2.14: Example of Decimal to Octal Conversion

Figure 2.15: Example of Decimal to Octal Conversion using Successive Division

OCTAL TO BINARY CONVERSION

In order to convert an octal number to a binary number we simply convert each digit of the octal number to its corresponding three- bit binary value, as shown in Fig.2.16.
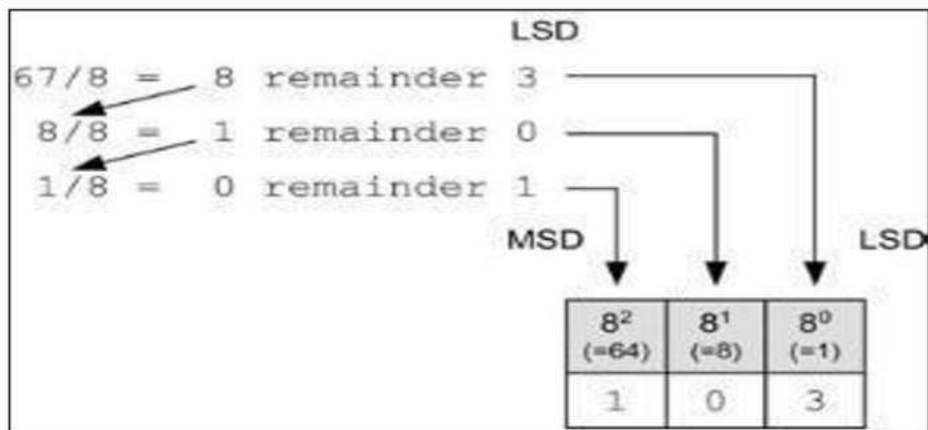

Figure 2.16: Example of Octal to Binary Conversion

BINARY TO OCTAL CONVERSION

Converting a binary number to its equivalent in octal is also extremely easy. In this case you simply need to arrange the binary number in groups of three binary digits from right to left and then convert each group to its equivalent octal number, as shown Fig. 2.17
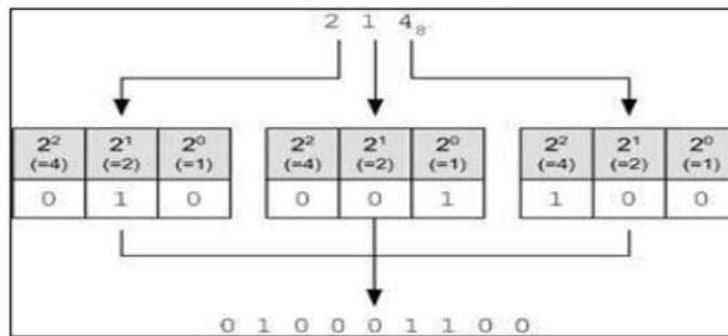

Figure 2.17 Example of Binary to Octal Conversion HEXADECIMAL NUMBERS

Although computers are quite comfortable working with binary numbers of 8, 16, or even 32 binary digits, humans find it inconvenient to work with so many digits at a time. The hexadecimal (base 16) numbering system offers a practical compromise acceptable to both to humans and to machines. One hexadecimal digit can represent four binary digits, thus an 8-bit binary number can be expressed using two hexadecimal digits. For example, 10000011 binary is the same as 83 when expressed in hexadecimal. The correspondence between a hexadecimal (hex) digit and the four binary digits it represents is quite straightforward and easy to learn (see Table2.2).

Note that, in hexadecimal, the decimal numbers from 10 to 15 are represented by the letters A to F respectively.

HEXADECIMAL TO DECIMAL CONVERSION

In order to convert a hexadecimal number to a decimal number we can determine the value of each successive hexadecimal digit, multiply it by the column value (in terms of the power of the base) and simply add the values up. For example, the hexadecimal number of A7 is converted by taking each digit and then multiplying it by the weight of the digit position, as shown in Figure 2.18.

Binary	Dec.	Hex.	Octal
0000	0	0	0
0001	1	1	1
0010	2	2	2
0011	3	3	3
0100	4	4	4
0101	5	5	5
0110	6	6	6
0111	7	7	7
1000	8	8	10
1001	9	9	11
1010	10	A	12
1011	11	B	13
1100	12	C	14
1101	13	D	15
1110	14	E	16
1111	15	F	17

Table 2.2: Binary, Decimal, Hexadecimal and Octal Numbers
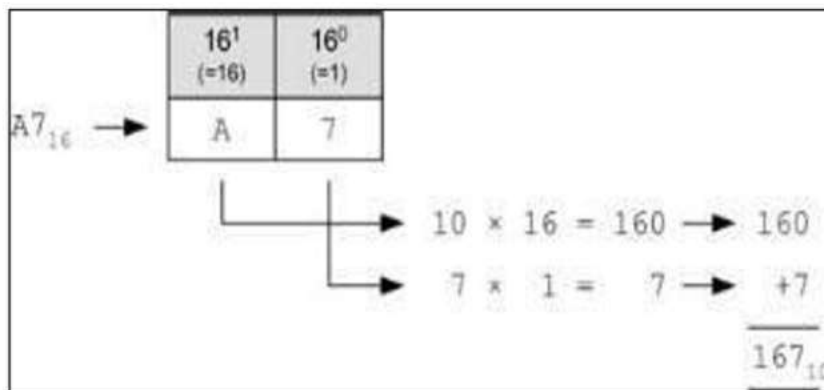
Fig 2.18: Example of Hexadecimal To Decimal Conversion

DECIMAL TO HEXADECIMAL TO CONVERSION

In order to convert a decimal number to its hexadecimal equivalent you can break the number down into a succession of numbers that are each powers of 16 and then place the relevant digit (a value between 0 and F) in the respective digit position, as shown in Figure 2.19. Note how, in the case of the example shown in Figure 2.19 (b) the letters F and E respectively replace the decimal numbers 15 and 14.
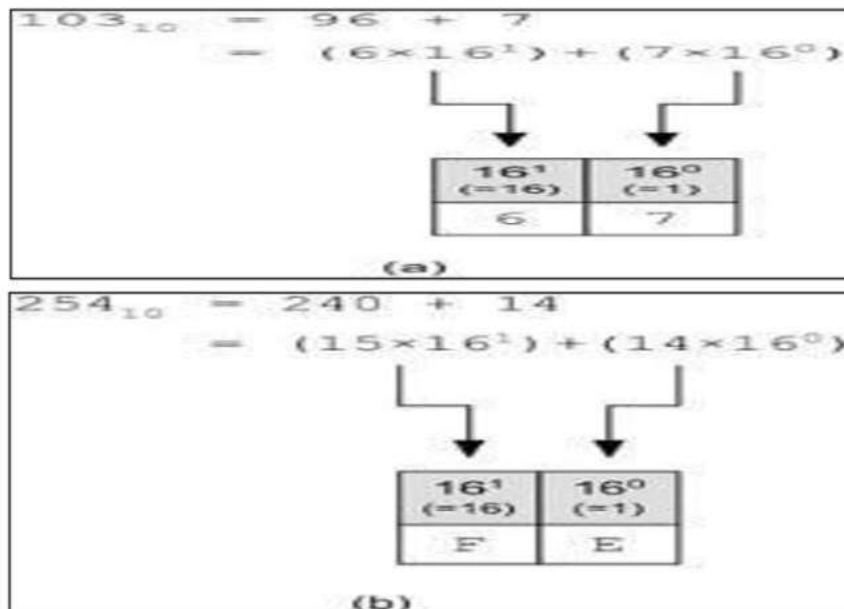
Figure 2.19 (a) & (b): Example of Decimal to Hexadecimal Conversion

HEXADECIMAL TO BINARY CONVERSION

In order to convert a hexadecimal number to a binary number we simply need to convert each digit of the hexadecimal number to its corresponding four-bit binary value, as shown in Figure 2.20.
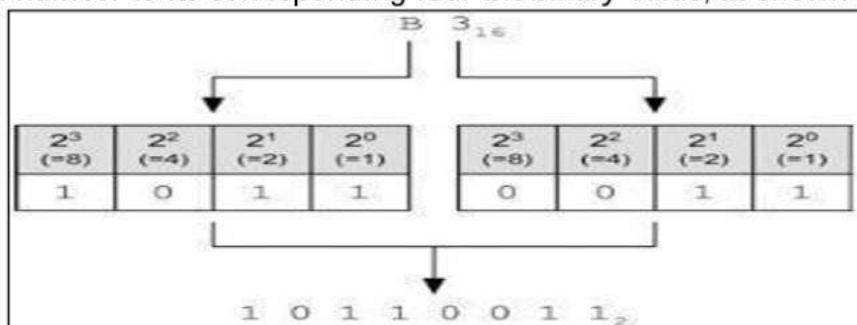
Figure 2.20: Example of Hexadecimal to Binary Conversion

BINARY TO HEXADECIMAL CONVERSION

Converting a binary number to its equivalent in hexadecimal is also extremely easy. In this case you simply need to arrange the binary number in groups of four binary digits working from right to left before converting each group to its hexadecimal equivalent, as shown Figure2.2

Figure 2.21: Example of Binary to Hexadecimal Conversion

5.3 DATA CONVERSION

INTRODUCTION

Because signals in the real world exist in both digital (on/off) and analogue (continuously variable) forms. Computer systems need to be able to accept and generate both types of signal as inputs and outputs respectively. Because of this, there is a need for devices that can convert signals in analogue form to their equivalent in digital form, and vice versa.
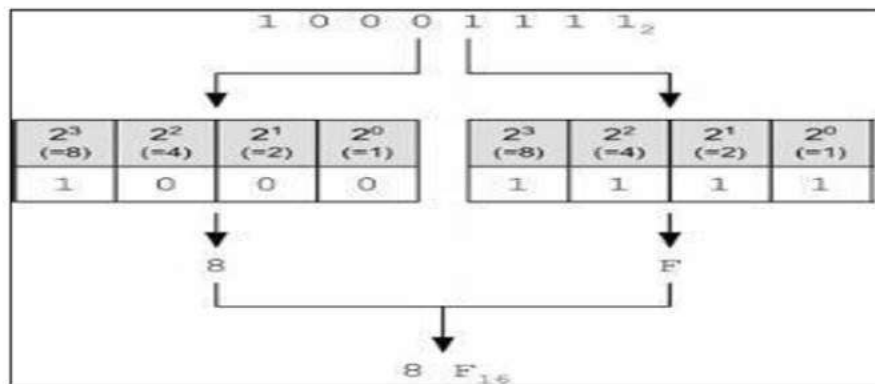
ANALOGUE AND DIGITAL SIGNALS/DATA

Examples of analogue and digital signals are shown in Figure 3.1. The analogue signal shown in Figure 3.1(a) consists of a continuously changing voltage level whereas the digital signal shown in Figure 3.1(b) consists of a series of discrete voltage levels that alternate between logic 0 ('low' or 'off') and logic 1 ('high' or'on').

The actual voltages used to represent the logic levels are determined by the type of logic circuitry employed however logic 1 is often represented by a voltage of approximately +5V and logic 0 by a voltage of 0V. In order to represent an analogue signal using digital codes it is necessary to approximate (or quantize) the signal into a set of discrete voltage levels as shown in Figure 3.2. The sixteen quantization levels for a simple analogue to digital converter using a four-bit binary code are shown in Fig. 3.4 above. Note that, in order to accommodate analogue signals that have both positive and negative polarity we have used the two's complement representation to indicate negative voltage levels. Thus, any voltage represented by a digital code in which the MSB is logic 1 will be negative. Figure 3.5 shows how atypical analogue signal would be quantized into voltage levels by sampling at regular intervals (t1, t2, t3, etc).
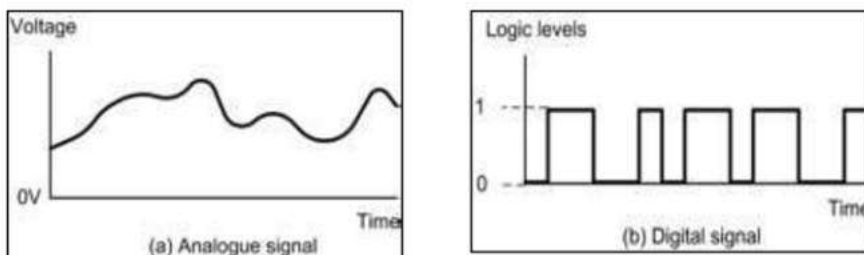
Figure 3.1 : Example of (a) Analogue and (b) Digital Signals
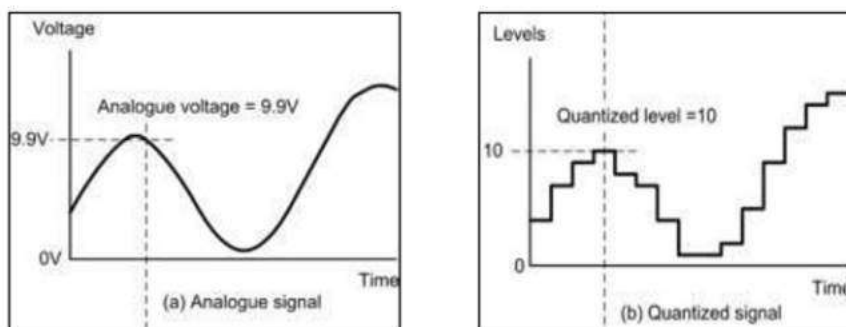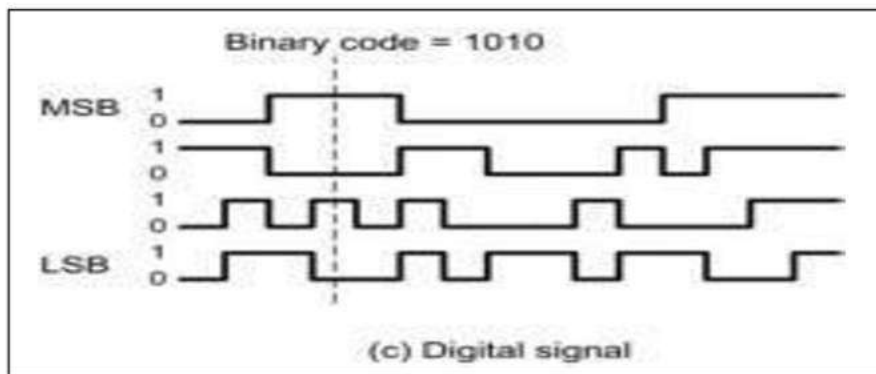
Figure 3.2: The process of quantizing an analogue signal into its digital equivalent

OPERATION OF DIGITAL TO ANALOGUE CONVERTER

The basic digital to analogue converter (DAC) has a number of digital inputs (often 8, 10, 12, or 16) and a single analogue output, as shown in Figure 3.3.
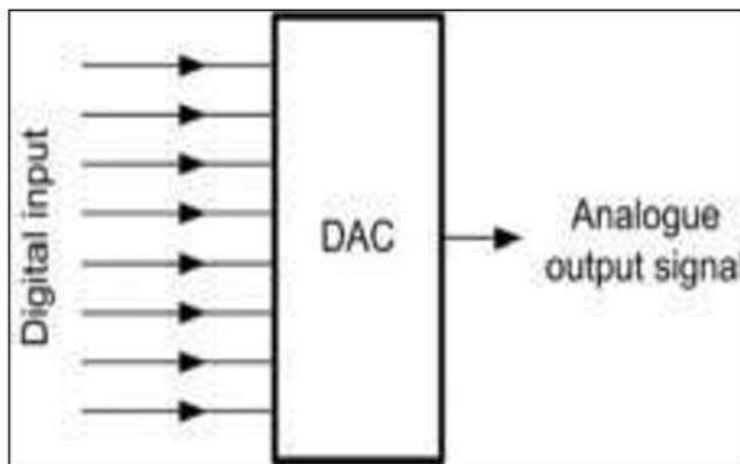
Figure 3.3: Basic DAC Arrangement
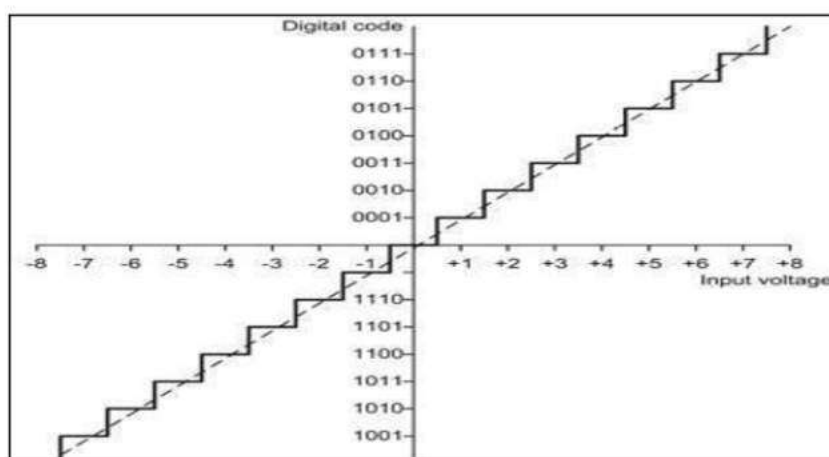
Figure 3.4: Quantization levels for a simple analogue to digital converter using a four – binary code

(Note the use of the two's complement to indicate negative voltage levels)

The simplest form of digital to converter shown in Fig. 3.6 below, buses a set of binary weighted resistors to define the voltage gain of an operational summing amplifier and a four-bit binary latch to store the binary input whilst it is being converted.
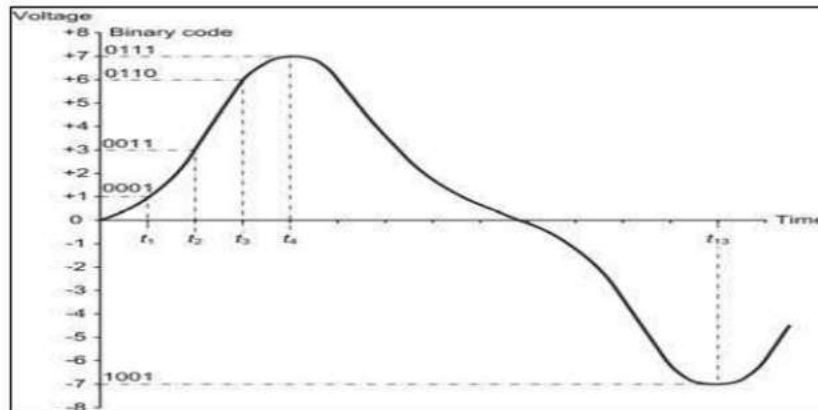
Figure 3.5: A bipolar analogue signal quantized into voltage levels by sampling intervals (t1, t2, t3, etc.)

Bit	Voltage gain
3 (MSB)	$-R/R = -1$
2	$-R/2R = -0.5$
1	$-R/4R = -0.25$
0 (LSB)	$-R/8R = -0.125$

Table 3.1: Voltage gain for the simple DAC

Bit 3	Bit 2	Bit 1	Bit 0	Output voltage
0	0	0	0	0V
0	0	0	1	−0.625V
0	0	1	0	−1.250V
0	0	1	1	−1.875V
0	1	0	0	−2.500V
0	1	0	1	−3.125V
0	1	1	0	−3.750V
0	1	1	1	−4.375V
1	0	0	0	−5.000V
1	0	0	1	−5.625V
1	0	1	0	−6.250V
1	0	1	1	−6.875V
1	1	0	0	−7.500V
1	1	0	1	−8.125V
1	1	1	0	−8.750V
1	1	1	1	−9.375V

Table 3.2: Output voltages produced by the simple DAC

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(a) Simple binary-weighted DAC
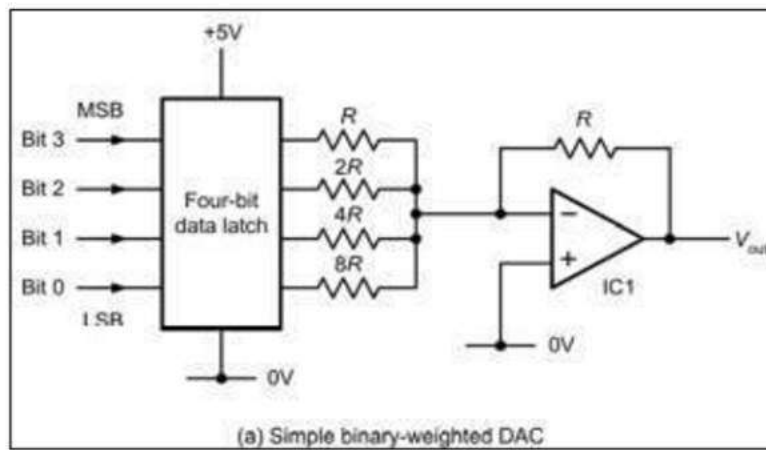
Figure 3.6: Simple DAV Arrangements

Note that, since the amplifier is connected in inverting mode, the analogue output voltage will be negative rather than positive. However, a further inverting amplifier stage can be added at the output in order to change the polarity if required. The voltage gain of the inputs to the operational amplifier (determined by the ratio of feedback to input resistance and taking into account the inverting configuration) is shown in Table 3.1. If we assume that the logic levels produced by the four-bit data latch are 'ideal' (such that logic 1 corresponds to +5V and logic 0 corresponds to 0V) we can determine the output voltage corresponding to the eight possible input states by summing the voltages that will result from each of the four inputs taken independently. For example, when the output of the latch takes the binary value 1010 the output voltage can be calculated from the relationship:

$$V_{out} = (-1 \times 5) + (-0.5 \times 0) + (-0.25 \times 5) + (-0.125 \times 0) = -6.25 \text{ V}$$

Similarly, when the output of the latch takes the binary value 1111 (the maximum possible) the output voltage can be determined from:

$$V_{out} = (-1 \times 5) + (-0.5 \times 5) + (-0.25 \times 5) + (-0.125 \times 5) = -9.375 \text{ V}$$

The complete set of voltages corresponding to all eight possible binary codes are given in the Table 3.2 above. An improved binary-weighted DAC This circuit operates on a similar principle but uses four analogue switches instead of a four-bit data latch. The analogue switches are controlled by the logic inputs so that the respective output is connected to the reference voltage (V_{ref}) when the respective logic input is at logic 1 and to 0V when the corresponding logic input is at logic 0. When compared with the previous arrangement, this circuit offers the advantage that the reference voltage is considerably more accurate and stable than using the logic level to define the analogue output voltage.

A further advantage arises from the fact that the reference voltage can be made negative in which case the analogue output voltage will become positive. Typical reference voltages are −5V, −10V, +5V and +10V.

Unfortunately, by virtue of the range of resistance values required, the binary weighted DAC becomes increasingly impractical for higher resolution applications. Taking a 10-bit circuit as an example, and assuming that the basic value of R is 1 kΩ, the binary weighted values would become as shown in Table 3.3 below. In order to ensure high accuracy, all of these resistors would need to be close-tolerance types (typically ±1%, or better). A more practical arrangement uses an operational amplifier in which the input voltage to the operational amplifier is determined by means of an R-2R

ladder, as shown in Figure3.7 below. Note that only two resistance values are required and that they can be any convenient value provided that one value is double the other.

Bit	Resistance
Bit 0	512 kΩ
Bit 1	256 kΩ
Bit 2	128 kΩ
Bit 3	64 kΩ
Bit 4	32 kΩ
Bit 5	16 kΩ
Bit 6	8 kΩ
Bit 7	4 kΩ
Bit 8	2 kΩ
Bit 9	1 kΩ

Table 3.3

(b) Improved binary-weighted DAC
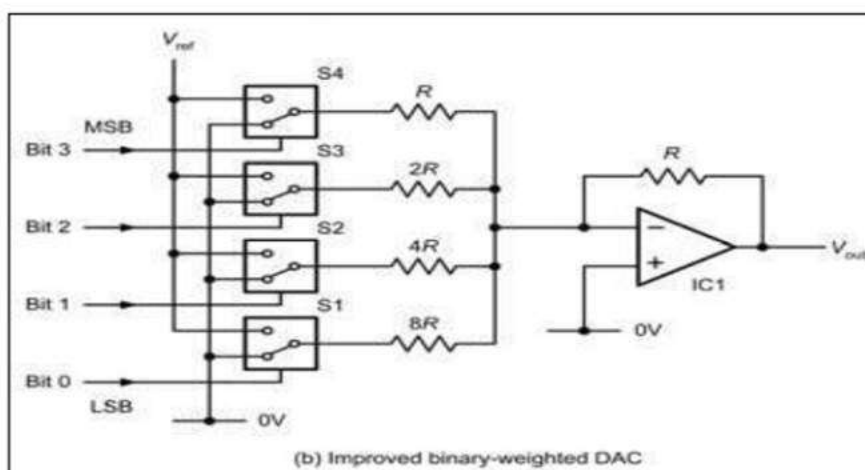
Figure 3.7: Simple DAV Arrangements relatively easy to manufacture matched resistances of close tolerance and high-stability on an integrated circuit chip).

OPERATION OF ANALOGUE TO DIGITAL CONVERSION

The basic analogue to digital converter (ADC) has a single analogue input and a number of digital outputs (often 8, 10, 12, or 16 lines), as shown in Figure 3.8.

Various forms of analogue to digital converter are available for use in different applications including multi-channel ADC with up to 16 analogue inputs. The simplest form of ADC is the flash converter shown in Figure 3.9. In this type of ADC the incoming analogue voltage is compared with a series of fixed reference voltages using a number of operational amplifiers (IC1 to IC7 in Figure3.10).

When the analogue input voltage exceeds the reference voltage present at the inverting input of a particular operational amplifier stage the output of that stage will go to logic 1. So, assuming that the

analogue input voltage is 2V, the outputs of IC1 and IC2 will go to logic 1 whilst the remaining outputs will be at logic 0. The priority encoder is a logic device that produces a binary output code that indicates the value of the most significant logic 1 received on one of its inputs. In this case, the output of IC2will be the most significant logic 1 and hence the binary output code generated will be 010 as shown in Figure 3.10 above. Flash ADC are extremely fast in operation (hence the name) but they become rather impractical as the resolution increases. For example, an 8- bit flash ADC would require 256 operational amplifier comparators and a 10-bit device would need a staggering 1,024 comparator stages. Typical conversion times for a flash ADC lie in the range 50 ns to 1 μs so this type of ADC is ideal for 'fast' or rapidly changing analogue signals.
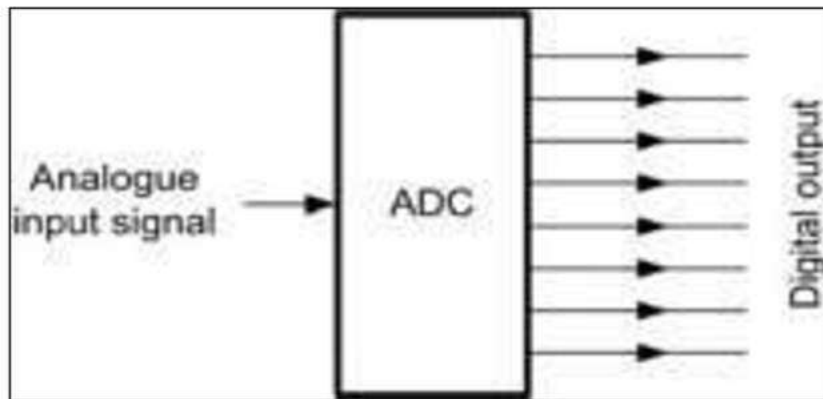

Figure 3.8: Basic ADC Arrangement
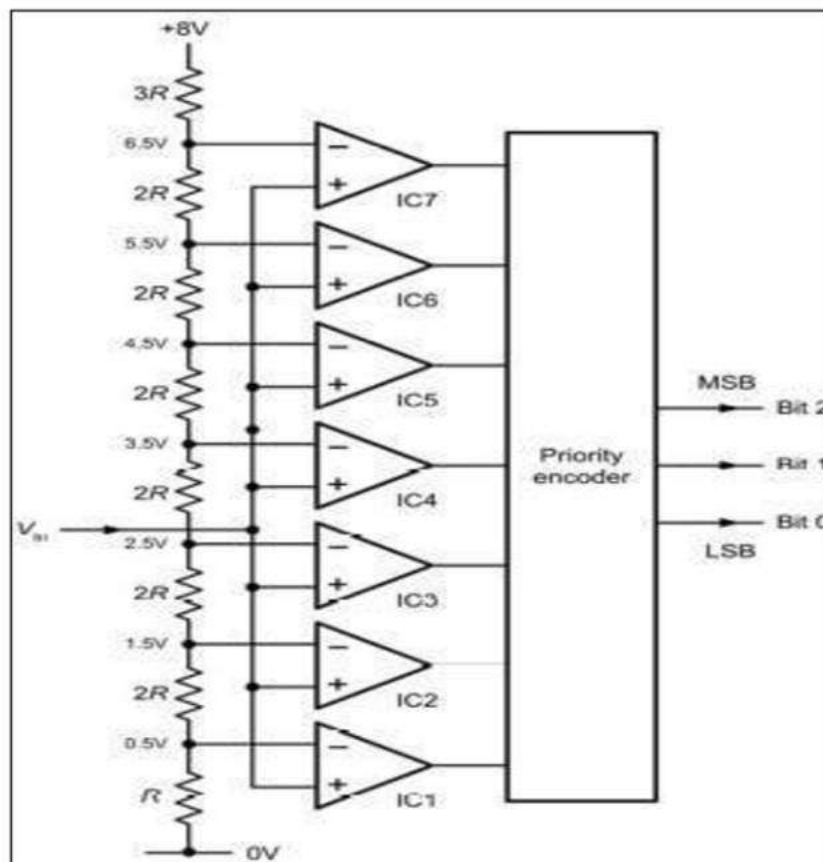
Figure 3.9: Simple Flash ADC

Input	Output		
	Bit 2	Bit 1	Bit 0
$V_{in} < 0.5V$	0	0	0
$0.5V < V_{in} < 1.5V$	0	0	1
$1.5V < V_{in} < 2.5V$	0	1	0
$2.5V < V_{in} < 3.5V$	0	1	1
$3.5V < V_{in} < 4.5V$	1	0	0
$4.5V < V_{in} < 5.5V$	1	0	1
$5.5V < V_{in} < 6.5V$	1	1	0
$V_{in} > 6.5V$	1	1	1

Figure 3.10

Due to their complexity, flash ADC are relatively expensive. A successive approximation ADC is shown in Figure 3.11. This shows an 8-bit converter that uses a DAC (usually based on an R- 2R ladder) together with a single operational amplifier compare at or (IC1) and a successive approximation register (SAR). The 8-bit output from the SAR is applied to the DAC and to an 8bit output latch. A separate end of conversion (EOC) signal (not shown in Fig. 3.12) is generated to indicate that the conversion process is complete and the data is ready for use.

When a start conversion (SC) signal is received, successive bits within the SAR are set and reset according to the output from the comparator. At the point at which the output from the comparator reaches zero, the analogue input voltage will be the same as the analogue output from the DAC and, at this point, the conversion is complete.

The end of conversion signal is then generated and the 8-bit code from the AR is read as a digital output code. Successive approximation ADC are significantly slower than flash types and typical conversion times (i.e. the time between the SC and EOC signals) are in the range 10 µs to 100 µs. Despite this, conversion times are fast enough for most non-critical applications and this type of ADC is relatively simple and available at low-cost. A ramp-type ADC is shown in Fig. 3.12.

Figure 3.11: A Successive Approximation ADC
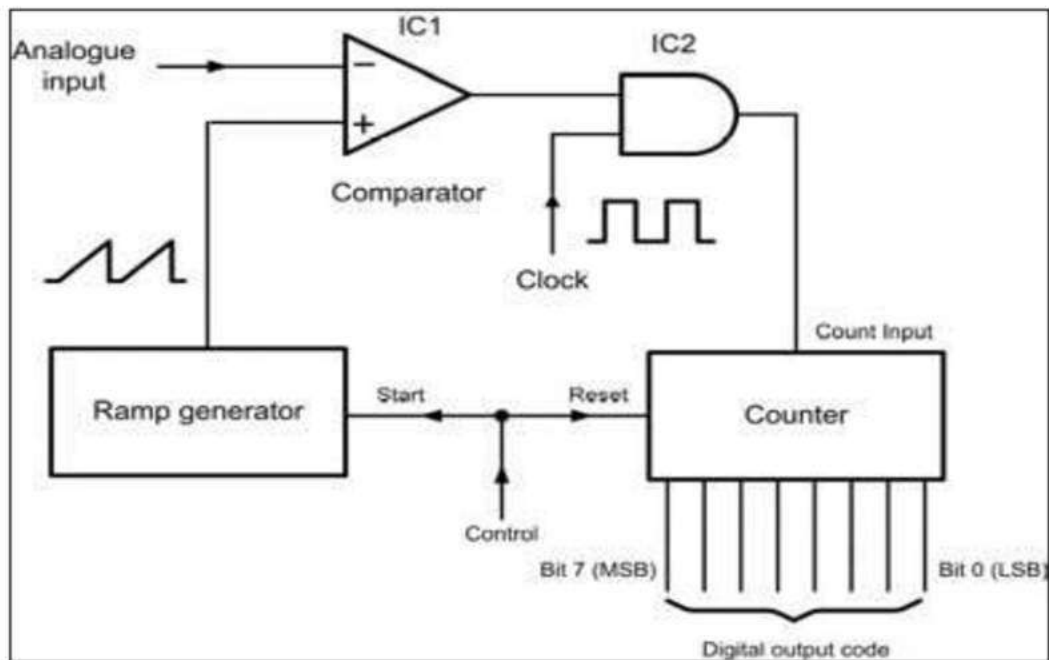
Figure 3.12 Ramp type ADC

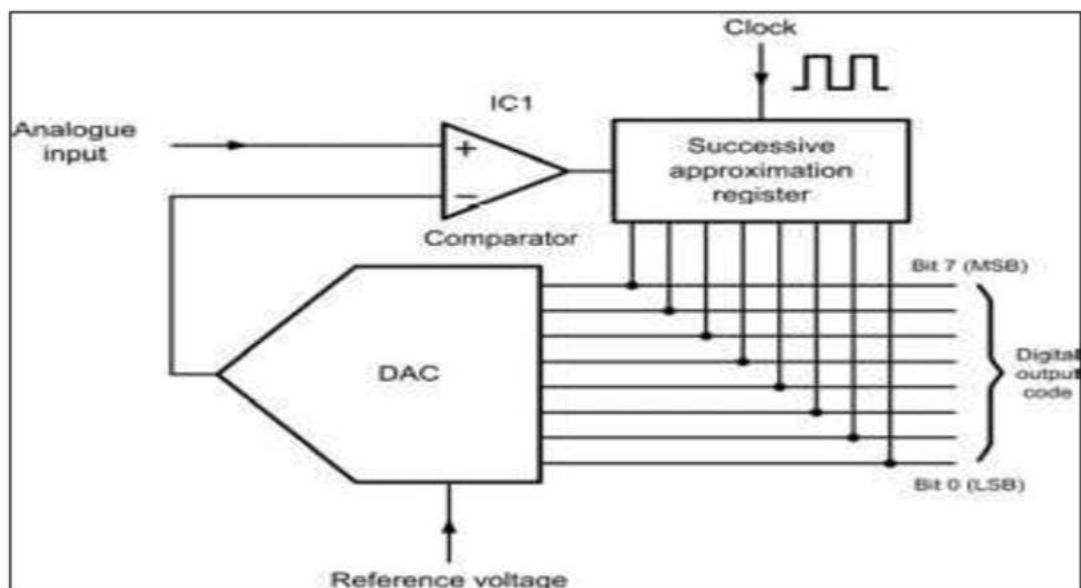This type of ADC uses a ramp generator and a single operational amplifier comparator, IC1. The output of the comparator (either a 1 or a 0 depending on whether the input voltage is greater or less than the instantaneous value of the ramp voltage). The output of the comparator is used to control a logic gate (IC2) which passes a clock signal (a square wave of accurate frequency) to the input of a pulse counter whenever the input voltage is greater than the output from the ramp generator. The pulses are counted until the voltage from the ramp generator exceeds that of the input signal, at which point the output of the comparator goes low and no further pulses are passed into the counter. The number of clock pulses counted will depend on the input voltage and the final binary count can thus provide a digital representation of the analogue input. Typical waveforms for the ramp-type waveform are shown in Fig.3.13.

Finally, the dual-slope ADC is a refinement of the ramp-type ADC which involves a similar comparator arrangement figure 3.14 above, but uses an internal voltage reference and an accurate fixed slope negative ramp which starts when the positive going ramp reaches the analogue input voltage. The important thing to note about this type of ADC is that, whilst the slope of the positive ramp depends on the input voltage, the negative ramp falls at a fixed rate. Hence this type of ADC can provide a very high degree of accuracy and can also be made so that it rejects noise and random variations present on the input signal. The main disadvantage, however, is that the process of ramping up and down requires some considerable time and hence this type of ADC is only suitable for 'slow' signals (i.e. those that are not rapidly changing).
Typical conversion times lie in the range 500µs to 20 ms.
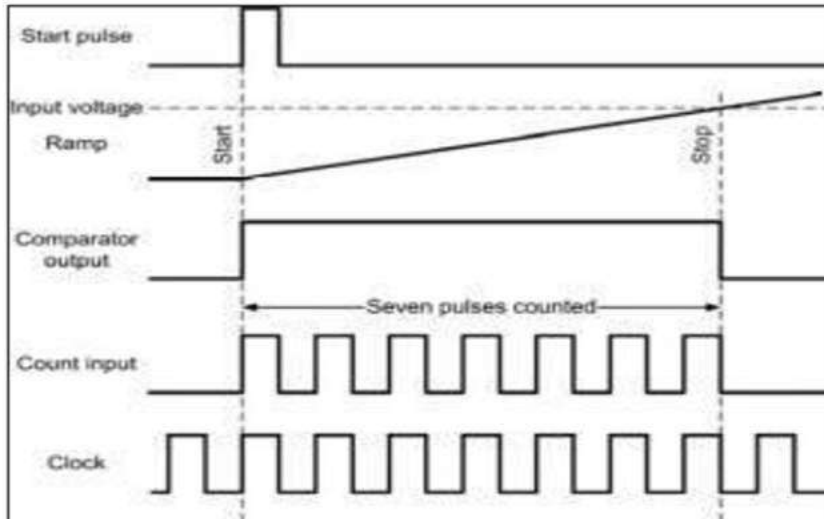
Figure 3.13: Waveforms for a Single-Ramp ADC
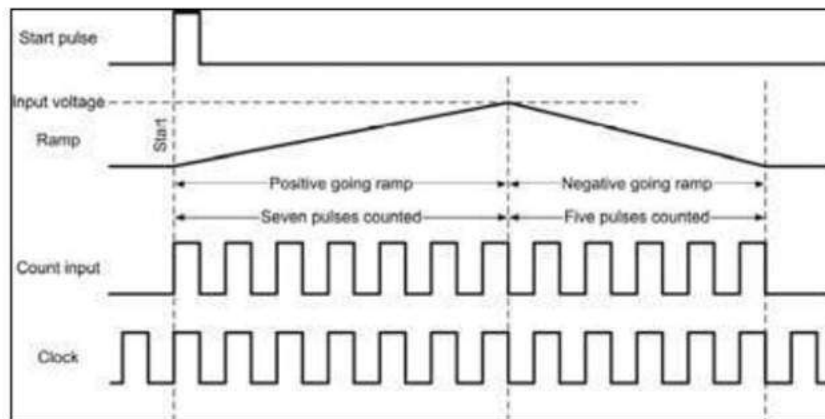
Figure 3.14: Waveforms for a Dual-Ramp ADC

LIMITATIONS OF VARIOUS TYPE OF CONVERSION

As previously discussed, analog signals are converted into digital signals so that the information is manipulated by instructions executed within a computer and then converted back to analog signals to drive analog display formats (such as hands on a clock) that are easily recognized by the crew. However, reconstructing a signal from digital-to-analog or from analog-to-digital can degrade the signal by introducing errors, also known as noise.

Reconstruction noise, as well as sampling noise from quantization, not only combine in the final signal, but also compound over multiple stages of conversion resulting in a loss of quality, or fidelity, of the original signal. All though not apparent, the waveform shown at the bottom of Figure 3-15 is a distorted version of the original waveform shown at the top. A prime example of an everyday device that converts analog signals to digital and back to analog signals is a telephone. The microphone on the phone receives sound pressure from the sender's voice, which produces an analog signal. The analog signal is converted to a digital signal which is then transmitted through the airwaves to the receiver's phone.
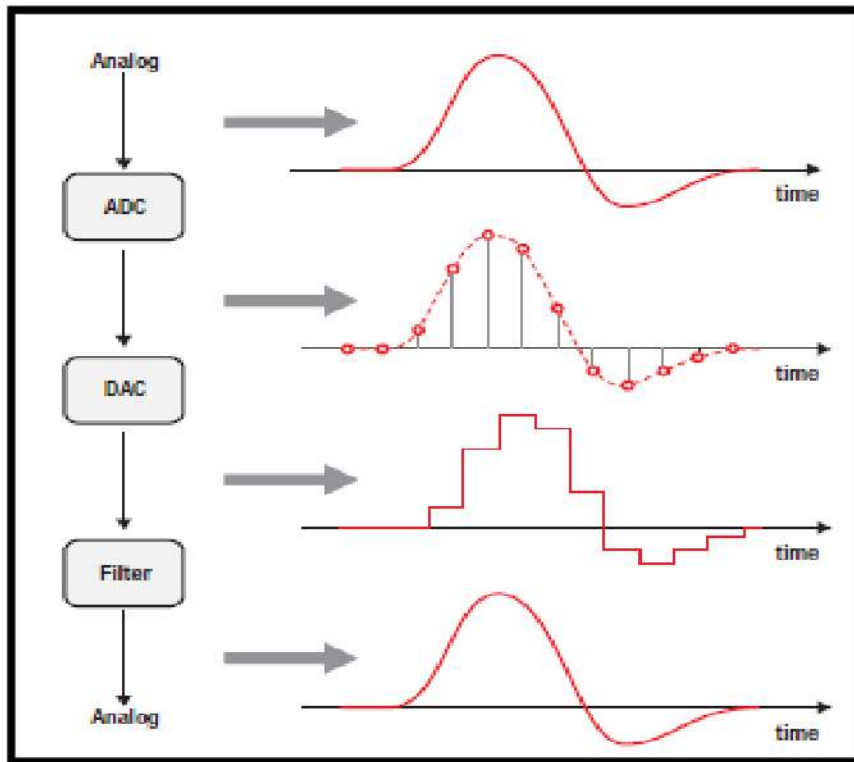
Figure 3.15: Conversion from analog to digital and back to analog

5.4 DATA BUS

INTRODUCTION

Data bus or transmission media is defined as a twisted shielded pair transmission line consisting of the main bus and a number of stubs. There is one stub for each terminal (system) connected to the by bus. The main data bus is terminated at each end with a resistance equal to the cable's characteristic impedance. This termination makes the data bus behave electrically like an infinite transmission line. Stubs, which are added to the main bus in order to connect the terminals, provide "local" loads, and produce an impedance mismatch where added. This mismatch, if not properly controlled, produces electrical reflections and degrades the performance of the main bus.

AIRCRAFT DATA BUS SYSTEMS:

These systems permit number of avionics equipment to communicate with one another and exchange data. These are two types:
1. Bidirectional (One Way)
2. Unidirectional (Two Way)

They can also be serial (one bit of data transmitted at a time) or parallel (where often 8, 16 or 32 bits of data appear as a group on a number of data lines at the same time). Because of the constraints imposed by conductor length and weight, all practical aircraft bus systems are based on serial (rather than parallel) data transfer. (Figure 4.1)

Bus systems provide an efficient means of exchanging data between the diverse avionic systems found in a modern aircraft as in Figure-4.2. Individual line replaceable units (LRU), such as the engine data interface or flap/slat electronics units shown in Fig.-4.3. , are each connected to the bus by means of a dedicated bus coupler and serial interface module (not shown in Fig. 4.3).

Within the LRU, the dedicated digital logic and microprocessor systems that process data locally each make use of their own local bus system. These local bus systems invariably use parallel data transfer which is ideal for moving large amounts of data very quickly but only over short distances.

(a) Unidirectional serial data

(b) Bidirectional serial data

(c) Unidirectional parallel data
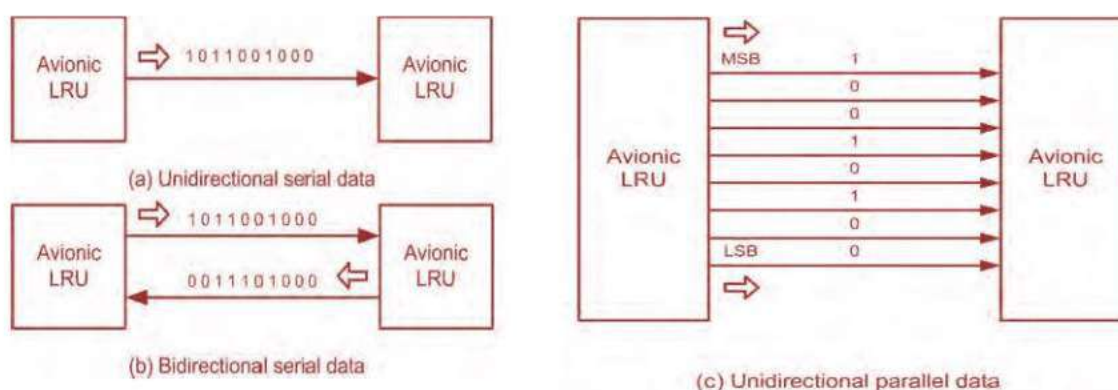
Figure4.1: Unidirectional & Bidirectional Serial & Parallel Data
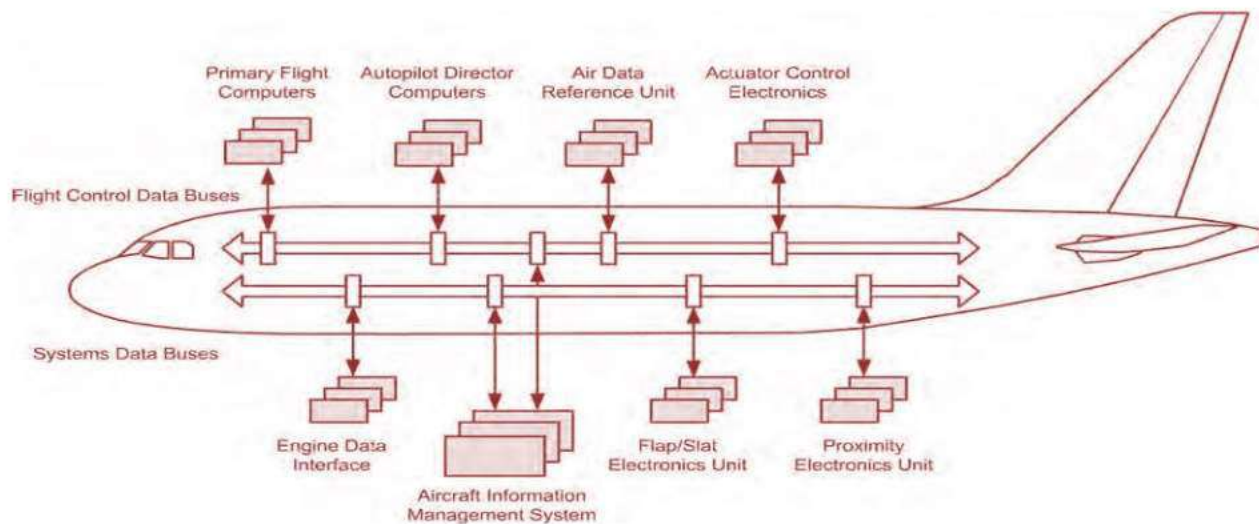
Figure 4.2 : Bus Systems Implemented on a Modern Passenger Aircraft

SERIAL BUS PRINCIPLES

A simple system for serial data transfer between two line replaceable units, each of which comprises an avionic system in its own right, is shown in Fig. 4.3. Within the LRU data is transferred using an internal parallel data bus (Either 8, 16, 32 or 64 bits wide).The link between the two LRUs is made using a simple serial cable (often with only two, four or six conductors). The required parallel-to-serial and serial-to-parallel data conversion is carried out by a bus interface (often this is a single card or module within the LRU). The data to be transferred can be synchronous (using clock signals generated locally within each LRU) or it may be asynchronous (i.e. self-clocking). The system shown in Fig.-4.3, has the obvious limitation that data can only be exchanged between two devices.

In practice we need to share the data between many LRU/avionic units. This can be achieved by the bus system illustrated in Fig.4.4. In this system, data is transferred using a shielded twisted pair (STP) bus cable with a number of coupler panels that are located at appropriate points in the aircraft (e.g. the flight deck, avionics bay, etc.).

Each coupler panel allows a number of avionic units to be connected to the bus using a stub cable. In order to optimize the speed of data transfer and minimize problems associated with reflection and mismatch, the bus cable must be terminated at each end using a matched bus terminator. Bus couplers are produced as either voltage mode or current mode units depending upon whether they use voltage or current sensing devices. Within each LRU/avionics unit, an interface is provided that performs the required serial-to-parallel or parallel-to serial data conversion, as shown in Fig.-4.5 & 4.6.
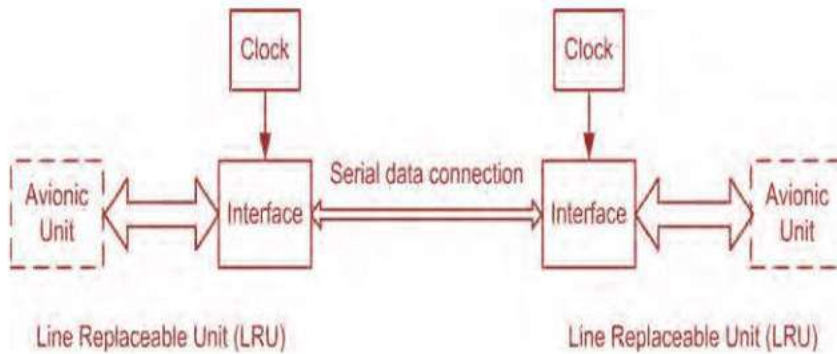
Figure 4.3 : A Simple System for Serial Data Transfer Between Two AvionicSystems
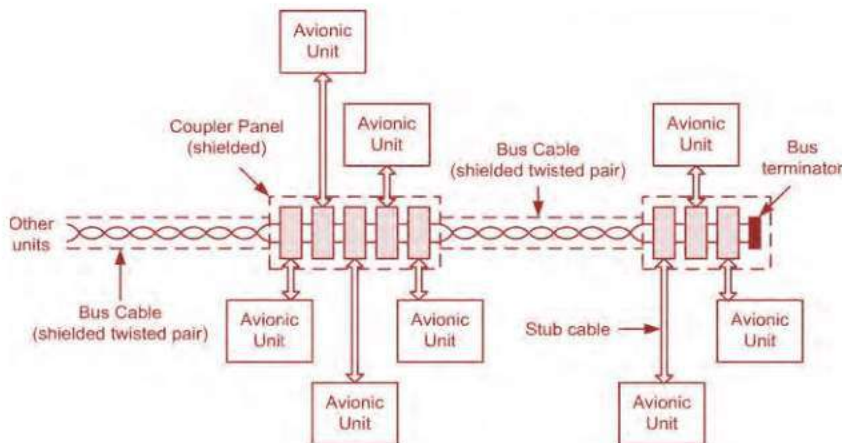
Figure 4.4 : A Practical Aircraft Data Bus

BUS CONTROLLER

The bus controller is responsible for directing the flow of data on the bus. While several terminals may be capable of performing as the bus controller, only one bus controller is allowed to be active at any one time. The bus controller is the only device allowed to issue commands onto the data bus. The commands may be for the transfer of data, or the control and management of the bus (referred to as mode commands).

Typically, the bus controller is a function that is contained within some other computer, such as a mission computer, a display processor, or a fire control computer. The complexity of the electronics associated with the bus controller is a function of the subsystem interface (the interface to the computer), the amount of error management and processing to be performed, and the architecture of the bus controller.

DESIGN FUNDAMENTALS

1. EQUIPMENT INTERCONNECTION

A single transmitter is connected with up to 20 data receivers via a single twisted and shielded pair of wires. The shields of the wires are grounded at both ends and at any breaks along the length of the cable. The shields are kept as short as possible.

2. MODULATION

Return-To-Zero (RZ) modulation is used. The voltage levels are used for this modulation scheme.

3. VOLTAGE LEVELS

The differential output voltages across the transmitter output terminal with no load is described in the table - 4.1:
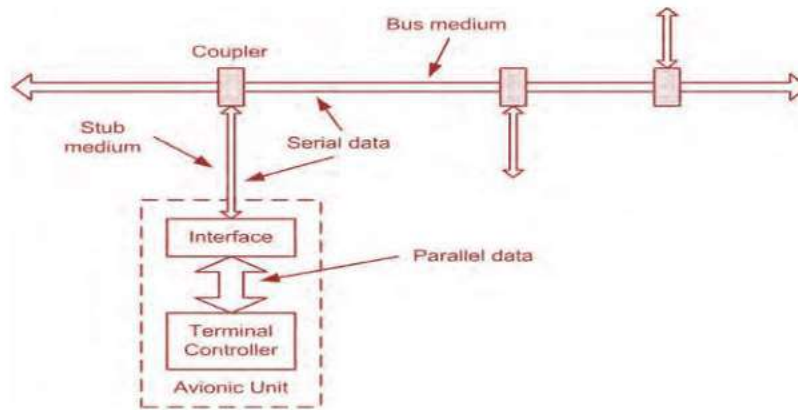
Figure 4.5 : A Basic Bus Interface
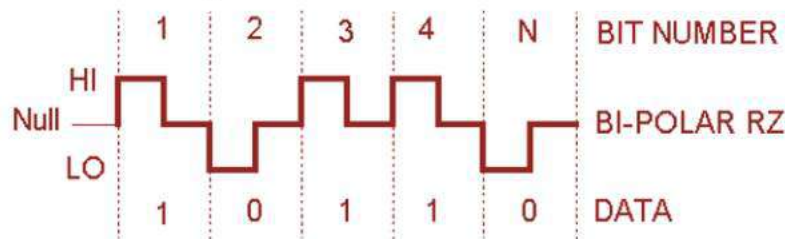
Figure4.6

	HI (V)	NULL (V)	LO (V)
Line A to Line B	+10 ± 1.0	0± 0.5	-10 ± 1.0
Line A to Ground	5± 0.5	0± 0.25	-5± 0.5
Line B to Ground	-5± 0.5	0± 0.25	5± 0.5

Table 4.1

ARINC SPECIFICATIONS

ARINC Specifications 419, 429, and 629 and Project Paper 453 are documents prepared by the Airlines Electronic Engineering Committee (AEEC) and published by Aeronautical Radio, Inc. These are among over 300 air transport industry avionics standards published since 1949. These documents, commonly referred to as ARINC 419, ARINC 429, ARINC 453, and ARINC 629, describe data communication systems used primarily on commercial transport airplanes. A limited

number of general aviation and military airplanes also use these data systems. The differences between the systems are described as follows.

ARINC 429

The ARINC 429 data bus has proved to be one of the most popular bus standards used in commercial aircraft. The ARINC 429 specification defines the electrical and data characteristics and protocols that are used. ARINC 429 employs a unidirectional data bus standard known as Mark 33 Digital Information Transfer System (DITS). Messages are transmitted in packets of 32-bits at a bit rate of either 12.5 or 100 kilobits per second (referred to as low and high bit rate respectively). Because the bus is unidirectional, separate ports, couplers and cables will be required when an LRU wishes to be able to both transmit and receive data. A typical data bus provides multidirectional transfer of data between multiple points over a single set of wires.

ARINC 429's simplistic one-way flow of significantly limits this capability, but the associated low cost and the integrity of the installations has provided the airlines with a system exhibiting excellent service for more than two decades. Note that a large number of bus connections may be required on an aircraft that uses sophisticated avionic systems. ARINC 429 has been installed on a wide variety of commercial transport aircraft including;

Airbus A310/A320 and 30/A340; Boeing 727, 737, 747, 757, and 767; and McDonnell Douglas MD-11. More modern aircraft (e.g. Boeing 777 & Airbus A380) use significantly enhanced bus specifications, in order to reduce the weight and size of cabling & to facilitate higher rates data than are possible with ARINC 429.

Despite these moves to faster, bidirectional bus standards, the ARINC 429 standard has proved to be highly reliable and so is likely to remain in service for many years to come. ARINC 429 is a two wire differential bus which can connect a single transmitter or source to one or more receivers. The term 'differential' simply means that neither of the two twisted wires is grounded and both convey signal voltages but of opposite polarity. This arrangement improves noise immunity which appears as a common mode signal induced on both of the conductors. Two bus speeds (High speed and low speed) are available and the data bus uses two signal wires to transmit 32 bit words. The ARINC 429 electrical characteristics are summarized in Table 4.2 below:

Voltage Levels	+ 5 V, 0 V, − 5 V (each conductor with respect to ground
Data Encoding	• Bi-polar return to zero
Word Size	• 32 bits
Bit Rate	• At High-Speed Operation bit rate of the system is 100 kilobits per second (kbps) ±1%. • At Low-Speed Operation the bit rate of the system is Within the range 12.0 to 14.5 kbps.

Table 4.2

NOTE The selected rate is maintained within 1%.

It is important to note that the received voltage on a serial bus depends on line length and the number of receivers connected to the bus. With ARINC 429, no more than 20 receivers should be connected to a single bus. Since each bus is unidirectional, a system needs to have its own transmit bus if it is required to respond or to send messages. Hence, to achieve bidirectional data transfer it is necessary to have two separate bus connections. Since there can be only one transmitter on a twisted wire pair, ARINC 429 uses a very simple, point-to- point protocol. The transmitter is continuously sending 32-bit data words or is placed in the NULL state. Note that although there may only be one receiver on a particular bus cable the ARINC specification supports up to 20. Other, faster and more sophisticated, bus systems are found on modern aircraft.

CLOCKING METHOD

Clocking is inherent in the data transmission. The identification of the bit interval is related to the initiation of either a HI or LO state from a previous NULL state in a bipolar RZ code. Transmission of sequential words is separated by at least four bit times of NULL (zero voltage). This eliminates the need for a separate clock signal and it makes the system self-clocking.

INFORMATION RATES

The minimum and maximum transmit intervals for each item of information are specific by ARINC Specification 429. Words with like labels but with different SDI codes are treated as unique items of information. Each and every unique item of information is transmitted once during an interval bounded in length by the specified minimum and maximum values. Stated another way, a data word having the same label and four different SDI codes will appear on the bus four times (once for each SDI code) during that time interval. Discrete bits contained within data words are transferred at the bit rate and repeated at the update rate of the primary data. Words dedicated to discretes should be repeated continuously at specified rates.

LONGEVITY OF ARINC 429

New airplane designs in the 21 century continue to employ the ARINC 429 bus for data transmission. The relative simplicity and integrity of the bus, as well as the ease of certification are characteristics that contribute to the continued selection of the ARINC 429 bus when the required data bandwidth is not critical. The ARINC 629 data bus developed as the replacement for ARINC 429 is used in applications where a large amount of data must be transferred or where many sources and sinks are required on a single bus.

ARINC 419

ARINC Specification 419, ''Digital Data Compendium,'' provides detailed descriptions of the various interfaces used in the ARINC 500 series of avionics standards prior to 1980. ARINC Specification 419 is often incorrectly assumed to be a standalone bus standard. ARINC Specification 419 provides a summary of electrical interfaces, protocols, and data standards for avionics built prior to the airlines' selection of a single standard, i.e., ARINC 429, for the distribution of digital information aboard aircraft.

ARINC 629

It supports a 20 Mbps data rate (20 times faster than ARINC 429), FDDI (Boeing's Fibre Distributed Data Interface), and 10 Mbps Ethernet. In FBW System, the ACEs (The Actuator Control Electronics) and PFCs (The Primary Flight Computer) communicate with each other, as well as with all other systems on the airplane, via triplex, bi-directional ARINC 629 Flight Controls data busses, referred to as L, C, and R. The connection from these electronic units to each of the data busses is via a stub cable and an ARINC 629 coupler. Each coupler may be removed and replaced without disturbing the integrity of the data bus itself.

COMMERCIAL STANDARD DIGITAL BUS (CSDB)

CSDB is one of three digital serial integration data buses that currently predominate in civilian aircraft. The CSBD finds its primary implementations in the smaller business and private General Aviation (GA) aircraft, but has also been used in retro fits of some commercial transport aircraft.

CSDB, a unidirectional data bus, was developed by the Collins General Aviation Division of Rockwell International. The bus used in a particular aircraft is determined by which company the airframe manufacturer chooses to supply the avionics. Collins is one of only a handful of major contributors to avionics today. CSDB is an asynchronous linear broadcast bus, specifying the use of a twisted, shielded pair cable for device interconnection.

Two bus speeds are defined in the CSDB specification. A low- speed bus operates at 12,500 bits per second (bps) and a high- speed bus operates at 50,000 bps. The bus uses twisted, terminated, shielded pair cable and has been tested to lengths of 50 m. The CSDB standard also defines other physical characteristics such as modulation technique, voltage levels, load capacitance, and signal rise and fall times. Fault protection for short-circuits of the bus conductors to both 28 VDC and 115 VAC is defined by the standard.

BASIC BUS OPERATION

CSDB standard has 3 types of transmissions, these are defined as :

1. CONTINUOUS REPETITION
Continuous repetition transmission refers to the periodic updates of certain bus messages. Some messages on CSDB are transmitted at a greater repetition rate than others. The CSDB standard lists these update rates, along with the message address and message block description.

2. NON CONTINUOUS REPETITION
Non-continuous repetition is used for parameters that are not always valid, or available, such as mode or test data. When non-continuous repetition transmission is in use, it operates the same as continuous repetition.

3. BURST TRANSMISSIONS
Burst transmission initiates an action (such as radio tuning), or may be used to announce a specific event. Operation in this mode initiates 16 repetitions of the action in each of 16 successive using an update rate of 20 per second. For CSDB, bytes consist of 11 bits: a start bit, 8 data bits, a parity bit, and a stop bit. The least significant bit (bit 0) follows the start bit. The CSDB standard defines the message block as "a single serial message consisting of a fixed number of bytes transmitted in a

fixed sequence." Essentially, a message block consists of a number of bytes concatenated together, with the first byte always being an address byte. A status byte may or may not be included in the message block. When it is, it immediately follows the address byte. The numbers of data bytes in a message block vary. Data are sent as frames consisting of a synchronization block followed by a number of message blocks. Figure-4.7 shows what transpires during a typical frame time.
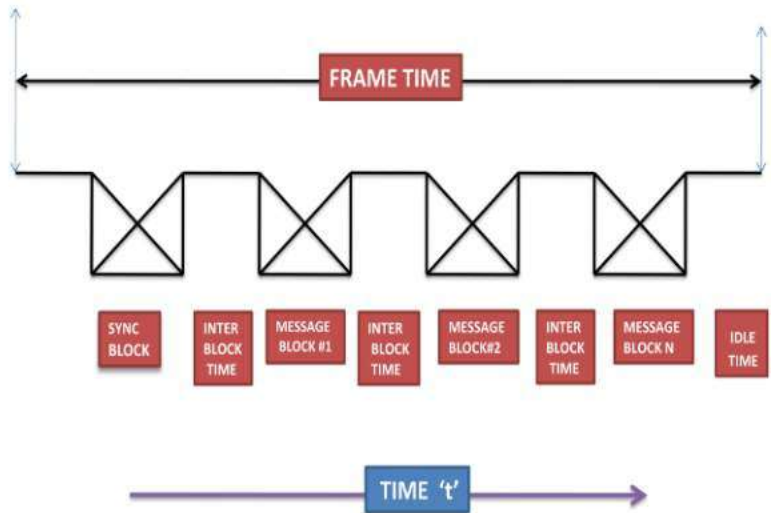
Figure 4.7

5.5   LOGIC CIRCUITS

LOGIC CIRCUIT GATE

A gate is a device that performs a basic operation on electrical signals. Gates are combined into circuits to perform more complicated tasks. There are three different, but equally powerful, notational methods for describing the behavior of gates and circuits. Aircraft logic systems follow the same conventions and standards as those used in other electronic applications. In particular, the MIL/ANSI standard logic symbols are invariably used and the logic elements that they represent operate in exactly the same way as those used in non-aircraft applications.

BUFFERS

Buffers do not affect the logical state of a digital signal (i.e. a logic 1 input results in a logic 1 output whereas a logic 0 input results in a logic 0 output). Buffers are normally used to provide extra current drive at the output but can also be used to regularize the logic levels present at an interface.

BOOLEAN EXPRESSIONS

Expressions in this algebraic notation are an elegant and powerful way to demonstrate the activity of electrical circuits. (Table 5.1 & 5.2)

Properties Of Boolean Algebra

$X + 0 = X$	$X . 1 = X$
$X + 1 = 1$	$X . 0 = 0$
$X + X = X$	$X . X = X$
$X + \overline{X} = 1$	$X . \overline{X} = 0$
$\overline{\overline{X}} = X$	

Table 5.1

Commutative	$X + Y = Y + X$	$XY = YX$
Associative	$X + (Y + Z) = (X + Y) + Z$	$X (YZ) = (XY) Z$
Distributive	$X (Y + Z) = XY + XZ$	$X + YZ = (X + Y) (X + Z)$
DeMorgan's	$\overline{X + Y} = \overline{X} . \overline{Y}$	$\overline{X . Y} = \overline{X} + \overline{Y}$

Table 5.2

A graphical representation of a circuit. Each type of gate is represented by a specific graphical symbol. Truth tables: Defines the function of a gate by listing all possible input combinations that the gate could encounter, and the corresponding output. There are six types of following gates NOT, AND, OR, XOR, NAND, NOR. The gates are distinguished only by their shape.

INDENTIFICATION OF COMMON LOGIC GATE SYMBOLS, TABLES & EQUIVALENT CIRCUIT

NOT GATE

A NOT gate accepts one input value and produces one output value. Figure 5.1, various representations of a NOT gate. By definition, if the input value for a NOT gate is 0, the output value is 1, and if the input value is 1, the output is 0. A NOT gate is sometimes referred to as an inverter because it inverts the input value.

AND GATE

An AND gate accepts two input signals. If the two input values for an AND gate are both 1, the output is 1; otherwise, the output is 0. Figure 5.2 has various representations of an AND gate.

$X = A.B$

Boolean Expression   **Logic Diagram Symbol**   **Truth Table**

$X = A'$
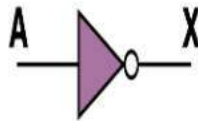
A	X
0	1
1	0

(a) Boolean expression, Symbol & truth table

(b) Series Circuit
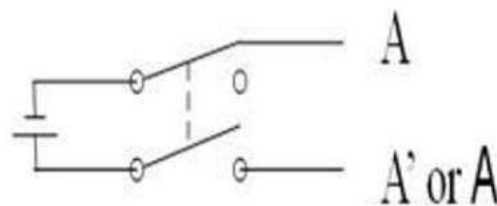
(c) Single – Throw Double – Pole Switch

(NOT) $\bar{X}$ 1   1   0   0
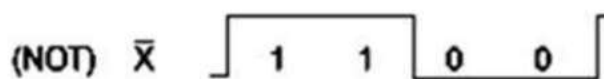
(d) Timing Diagram

Figure5.1: For NOT gate

Boolean Expression   **Logic Diagram Symbol**   **Truth Table**

$$X = A \cdot B$$

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(a) Boolean expression, Symbol & truth table

(AND) X Y ▸ 0   0   0   1
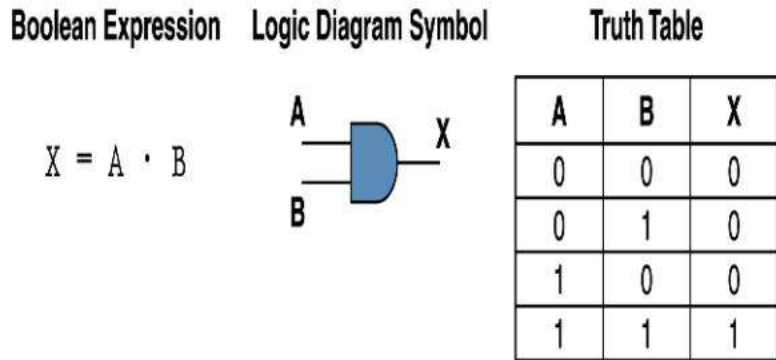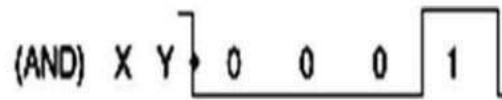
(b) Timing Diagram

Figure 5.2: For AND Gate

NAND GATE

This gate opposite of the AND gate. Figure 5.3, has various representations of a NAND gate

Boolean Expression   **Logic Diagram Symbol**   **Truth Table**

$$X = (A \cdot B)'$$

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0
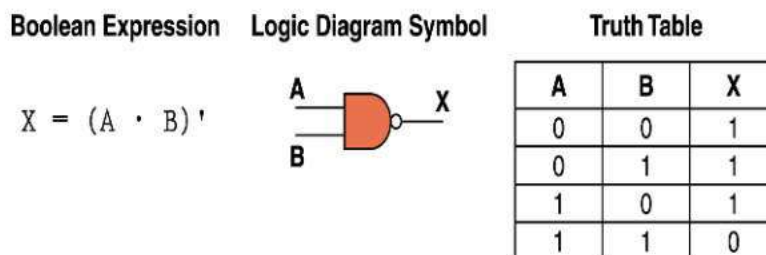
AND GATES WITH MORE INPUTS

Gates can be designed to accept three or more input values. A three-input AND gate, for example, produces an output of 1 only if all input values are 1. Figure 5.4, various representations of a three-input AND gate.

Boolean Expression   **Logic Diagram Symbol**   **Truth Table**

$$X = A \cdot B \cdot C$$

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1
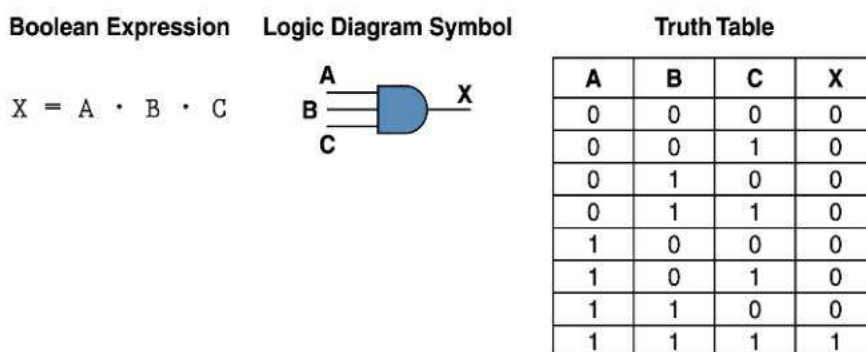
OR GATE

If the two input values are both 0, the output value is 0; otherwise, the output is 1. Figure-5.5, shows various representations of a OR gate
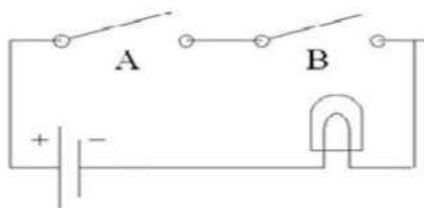

| | Boolean Expression | Logic Diagram Symbol | Truth Table |

Boolean Expression   **Logic Diagram Symbol**   **Truth Table**

$$X = A + B$$

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1
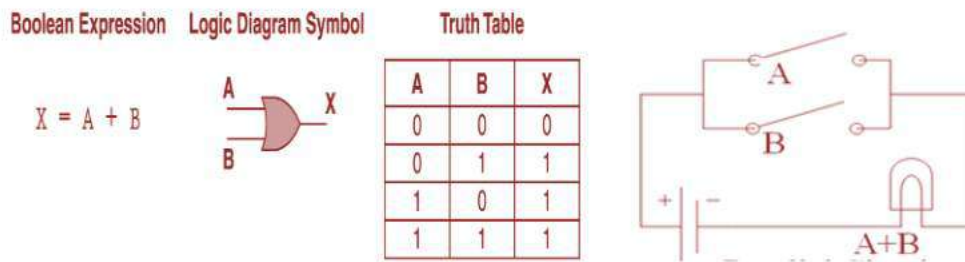
Figure 5.5 OR Gate with 2 input.

NOR GATES

These gates are essentially the opposite of the OR Gate. Figure 5.6, various representations of a NOR gate

XOR GATE

An XOR gate produces 0 if its two inputs are the same, and a 1 otherwise. Note the difference between the XOR gate and the OR gate; they differ only in one input situation. When both input signals are 1, the OR gate produces a 1 and the XOR produces a 0. Figure 5.7, various representations of an XOR gate.

GATE'S CONSTRUCTION

A transistor is a device that acts, depending on the voltage level of an input signal, either as a wire that conducts electricity or as a resistor that blocks the flow of electricity. A transistor has no moving parts, yet acts like a switch. It is made of a semiconductor material, which is neither a particularly good conductor of electricity, such as copper, nor a particularly good insulator, such as rubber. A transistor has three terminals, A Collector, A base and an emitter typically connected to a ground wire. If the electrical signal is grounded, it is allowed to flow through an alternative route to the ground (literally) where it can do no harm. Figure 5.8

It turns out that, because the way a transistor works, the easiest gates to create are the NOT, NAND and NOR gates, Figure 5.9.

Boolean Expression   **Logic Diagram Symbol**   **Truth Table**

$$X = (A + B)'$$

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0
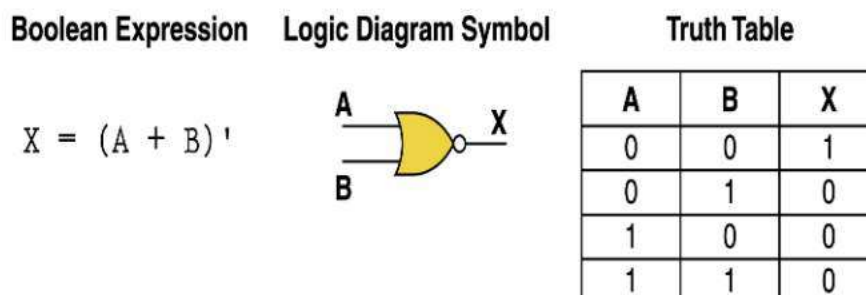
Figure 5.6: NOR Gate

Boolean Expression	Logic Diagram Symbol	Truth Table		

$$X = A \oplus B$$
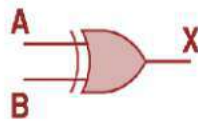
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Figure 5.7: XOR Gate
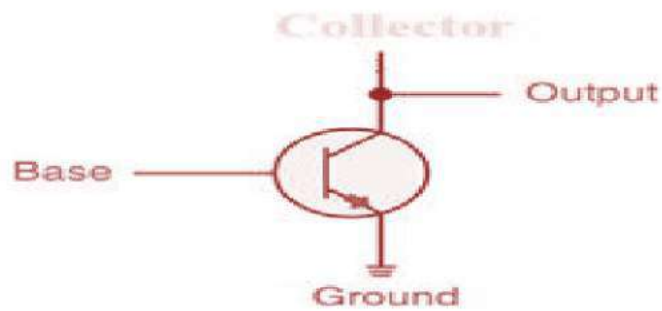
Figure 5.8: Transistor
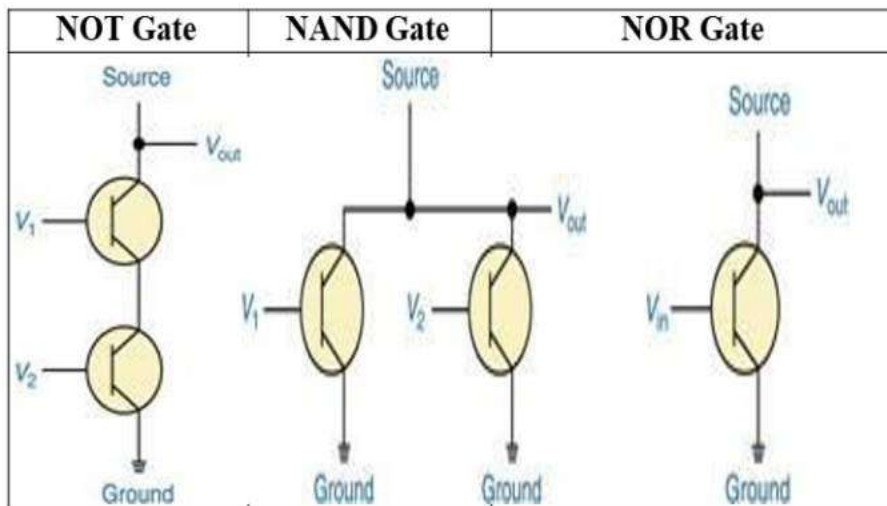
Figure 5.9: Construction of Gates by Using Transistors

LOGICAL OPERATIONS WITH NANDGATES
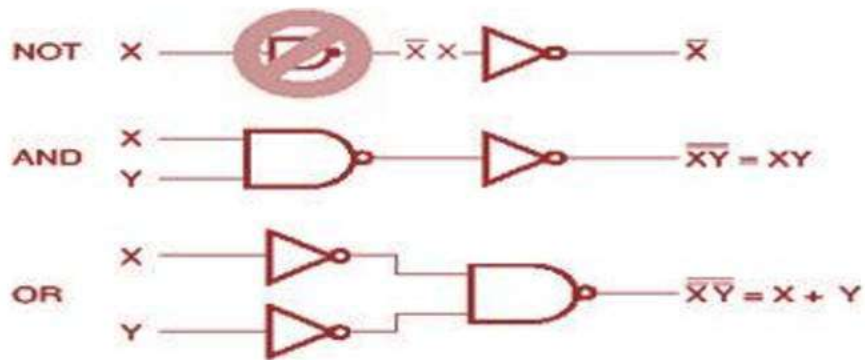
Figure5.10

ALTERNATIVE GRAPHICS SYMBOLS FOR NAND AND NOT GATES

(a) AND - NOT

(b) NOT – OR

(c) NOT
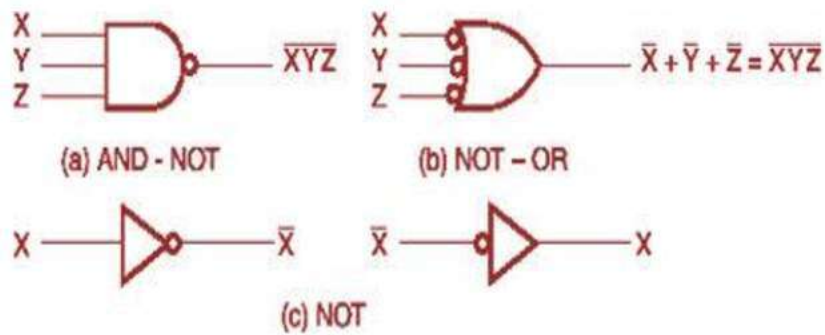
Figure5.11

LOGICAL OPERATIONS WITH NOR GATES

Figure5.12

(a) OR – NOT   (b) NOT – AND
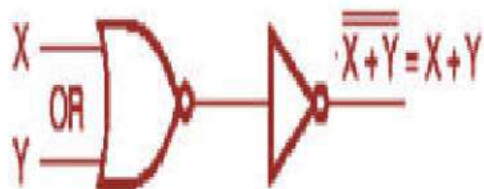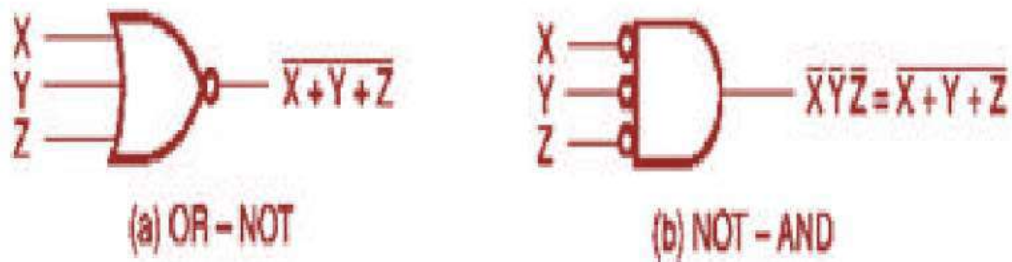
Figure5.13

DEMONSTRATION OF POSITIVE AND NEGATIVELOGIC

X	Y	Z
L	L	L
L	H	L
H	L	L
H	H	H

(a) Truth table with H and L

(b) Gate block diagram

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

(c) Truth table for positive logic

(d) Positive-logic AND gate

X	Y	Z
1	1	1
1	0	1
0	1	1
0	0	0

(e) Truth table for negative logic

(f) Negative-logic OR gate

Figure5.14

$F = X \oplus Y$

Figure5.15

50
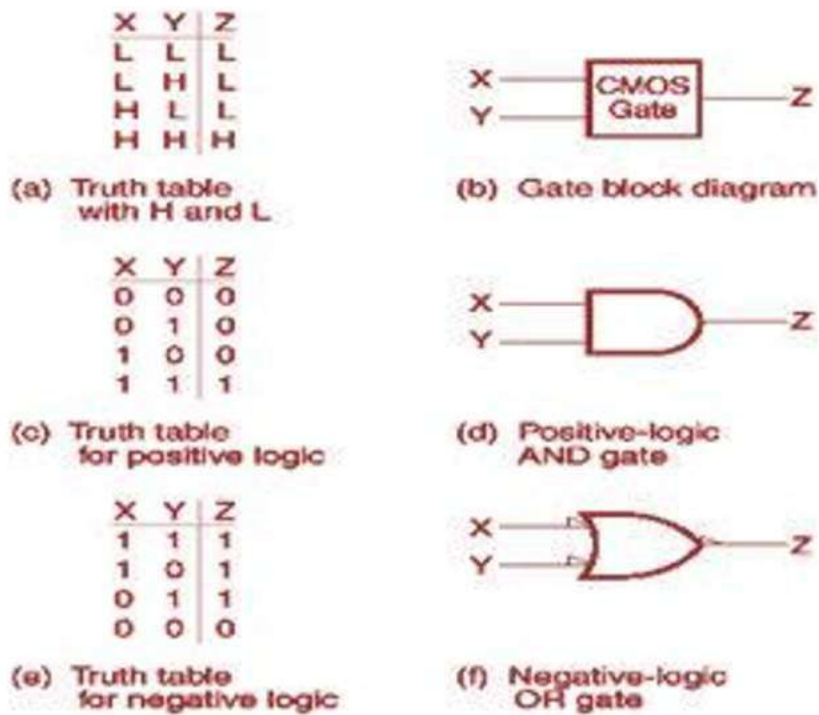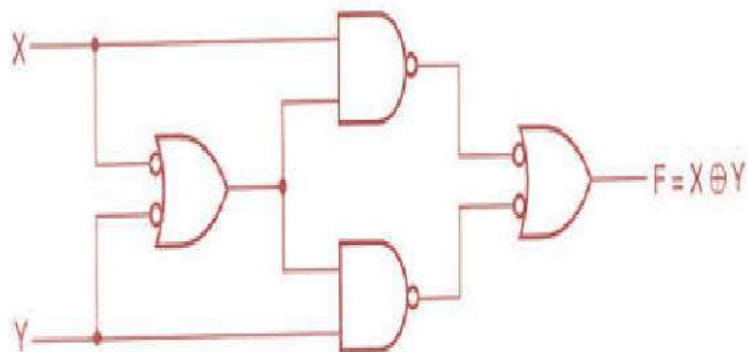
COMBINATIONAL CIRCUITS

Gates are combined into circuits by using the output of one gate as the input for another.
For Example
1. Because there are three inputs to this circuit, eight rows are required to describe all possible input combinations. This circuit using Boolean algebra: (Figure 5.16(a) & Truth Table below)
(AB + AC)
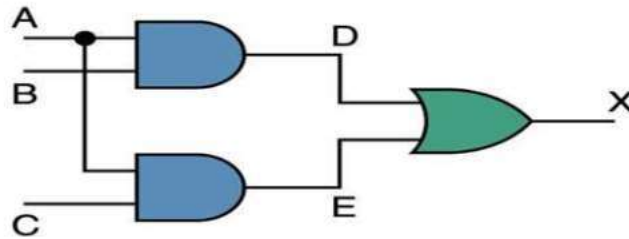
Figure5.16 (a)

A	B	C	D	E	X
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

Figure 5.16(a) Truth table

2. Now consider another following Boolean expression: (Figure5.17 & Truth Table 5.18 below)
A (B + C)
Now compare the final result column of both truth tables. We have found that they are identical and both circuits produce the exact same output for each input value combination. Hence Boolean algebra allows us to apply provable mathematical principles to help us design logical circuits.
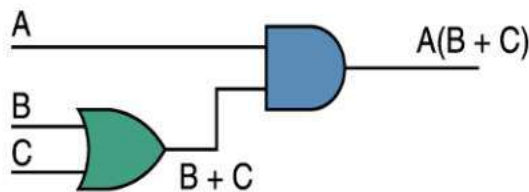
Figure5.17

A	B	C	B + C	A(B+C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Figure 5.18

APPLICATION OF LOGIC GATES IN AIRCRAFT SYSTEM

LANDING GEAR WARNING LOGIC

Now let's look at a more practical example of the use of logic in the typical aircraft system shown in Figure 5.19. The inputs to this logic system consist of five switches that detect whether or not the respective landing gear door is open. The output from the logic system is used to drive six warning indicators. Four of these are located on the overhead display panel and show which door (or doors) are left open whilst an indicator located on the pilot's instrument panel provides a master landing gear door warning. A switch is also provided in order to enable or disable the five door warning indicators.

The landing gear warning logic primary module consists of the following integrated circuit devices: (Table 5.3)

A1	Regulated Power Supply for A5
A2	Regulated Power Supply for A7 and A11
A5	Ten Inverting (NOT) Gates
A7	Five – Input NAND Gate
A11	Six Inverting (NOT) Gates

Table 5.3

Note that the power supply for A1 and A2 is derived from the essential services DC bus. This is a 28V DC bus which is maintained in the event of an aircraft power failure. Note also that the indicators are active-low devices (in other words, they require a logic 0 input in order to become illuminated).
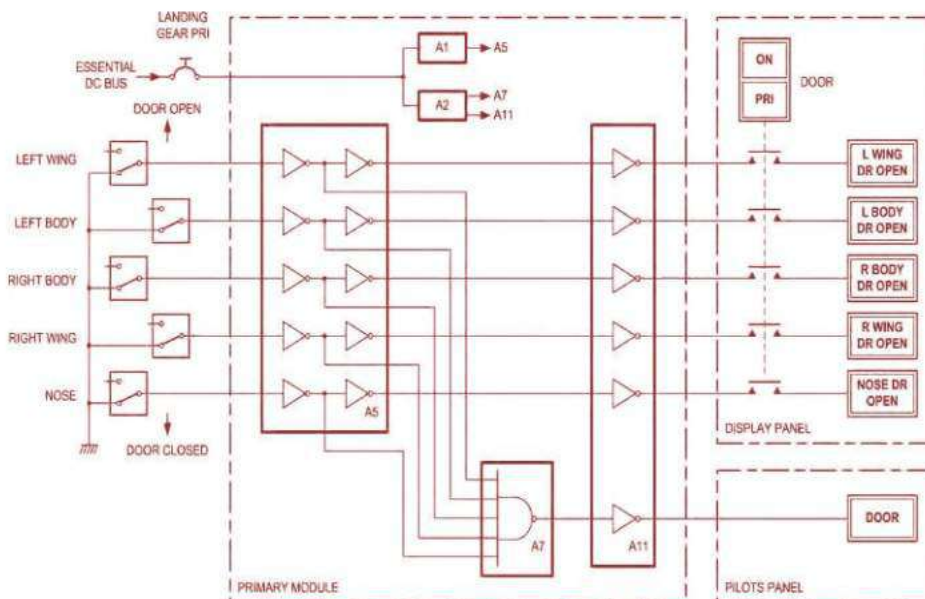
Figure 5.19: Landing Gear Warning Logic

APU STARTER LOGIC

An example of the use of a monostable is shown in the auxiliary power unit (APU) starter logic shown in Figure 5.20. This arrangement has three inputs (APU START, APU SHUTDOWN, and APU RUNNING) and one output (APU STARTER MOTOR). The inputs are all active-high (in other words, a logic 1 is generated when the pilot operates the APU START switch, and so on). The output of the APU starter motor control logic goes to logic 1 in order to apply power to the starter motor via a large relay.

There are a few things to note about the logic arrangement shown in Figure 5.21:

1. When the APU runs on its own we need to disengage the starter motor. In this condition the APU MOTOR signal needs to become inactive (i.e. it needs to revert to logic 0).

2. We need to avoid the situation that might occur if the APU does not start but the starter motor runs continuously (as this will drain the aircraft batteries). Instead, we should run the starter motor for a reasonable time (say, 60 seconds) before disengaging the starter motor. The 60 second timing is provided by means of a positive edge triggered monostable device. This device is triggered from the APU START signal.

3. Since the pilot is only required to momentarily press the APU START switch, we need to hold the condition until such time as the engine starts or times out (i.e. at the end of the 60 second period). We can achieve this by OR'ing the momentary APU START signal with the APU STARTER MOTOR signal.

4. We need to provide a signal that the pilot can use to shut down the APU (for example, when the aircraft's main engines are running or perhaps in the event of a fault condition). In order to understand the operation of the APU starter motor logic system we can once again trace through the logic system using 1's and 0's to represent the logical condition at each point (Just as we did for landing gear door warning logic). In Fig. 5.22 the APU is in normal flight and the APU is not running. In this condition the main engines are providing the aircraft's electrical power.

In Figure 5.22 the pilot is operating the APU START switch. The monostable is triggered and output of the OR and AND gates both go to logic 1 in order to assert the APU STARTER MOTOR signal.

The APU START signal is removed but the output of the AND gate is held at logic 1 by feeding back its logical state via the OR gate. The mono-stable remains triggered and continues to produce logic 1 output for its 60 second period. The APU is now running and the APU RUNNING signal has gone to logic 1 in order to signal this conditions. This results in the output of the AND gate going to logic 0 and the APU STARTER MOTOR signal is no longer made active. The starter motor is therefore disengaged. In the APU has failed to run during the 60 second mono-stable period. In this timed out condition the output of the AND gate goes to logic 0 and the APU
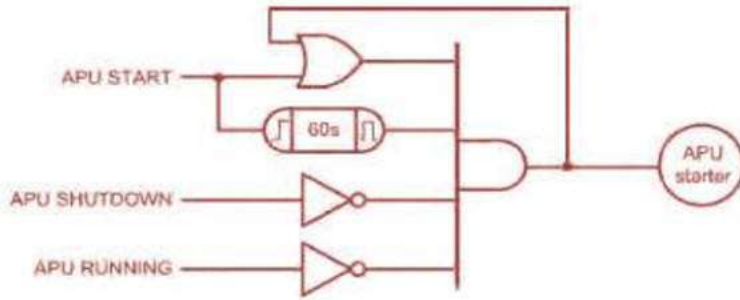
Figure 5.20 : APU Starter Logic
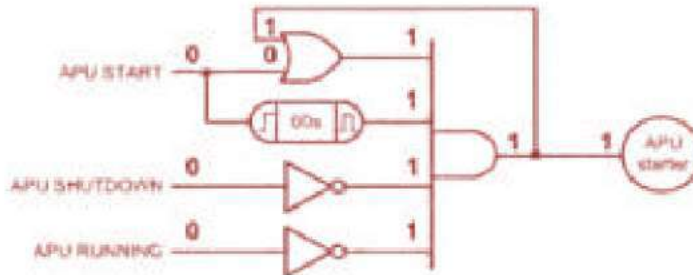
Figure 5.21: APU Starter Motor Continues to Run for Up to 60s (APU Starter Operation Continues)
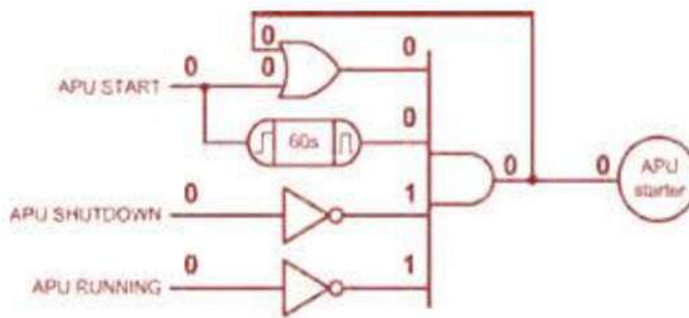
Figure 5.21: Normal Flight, Engine Power Generation, APU Not Running (APU Starter Operation)
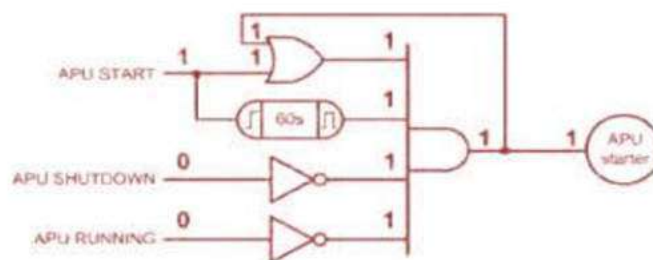
Figure 5.22: APU Starter Switch Operated; APU Starter Motor Begins to Run (APU Starter Operation)
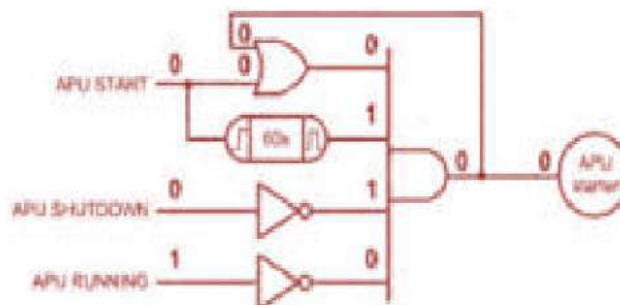
Figure 5.23: APU Runs Before 60s Timeout; Starter Motor Stops When APU Runs (APU Starter Operation Continues)

INTERPRETATION OF LOGIC DIAGRAM

ADDERS

At the digital logic level, addition is performed in binary. Addition operations are carried out by special circuits called, appropriately, adders. The result of adding two binary digits could produce a carry value.

A circuit that computes the sum of two bits and produces the correct carry bit is called a half adder.

1. FULL ADDER (Figure 5.23&Truth Table below)

A	B	Carry-in	Sum	Carry-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
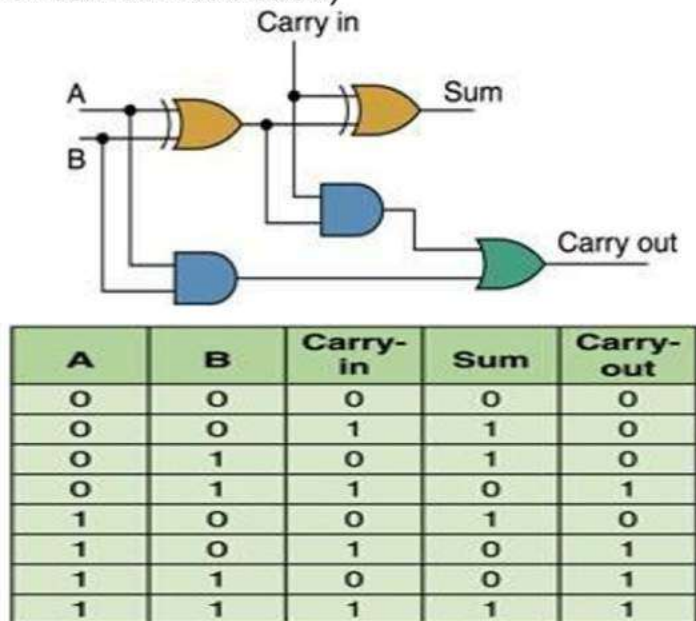
Figure 5.23: Full Adder with Truth Table
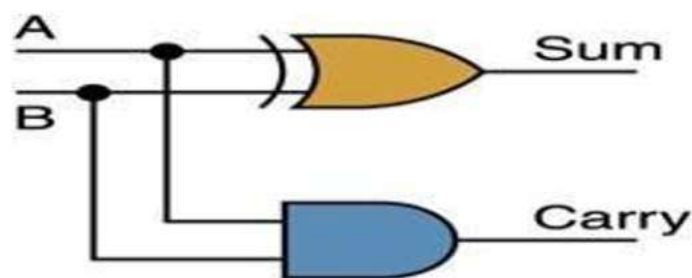
Logic Diagram

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 5.24 : Half Adder with Truth Table

5.6 BASIC COMPUTER STRUCTURE

INTRODUCTION

Computer is a device that transforms data into meaningful information. Computer can also be defined in terms of functions it can perform. A computer can

- Accept data,
- Store data,
- Process data as desired, and
- Retrieve the stored data as and when required.
- Print the result in desired format.

The major characteristics of a computer are high speed, accuracy, diligence, versatility and storage. Computers can be generally classified by size and power as follows, though there considerable overlap:

1. PERSONAL COMPUTER
2. SUPER COMPUTER
3. MINI COMPUTER
4. WORK STATION COMPUTER
5. MICRO COMPUTER

COMPUTER ARCHITECTURE / COMPUTER TERMINOLOGY

It is single chip consist of three parts which includes an arithmetic logic unit (ALU), temporary storage registers, central processing unit, computer is the arrangement of its internal subsystems: the microprocessor(s), memory, I/O and interfacing. Each subsystem may be concentrated on a single IC or spread between many chips. These are detailed in following Paragraphs: [Figure 6.1].

THE CENTRAL PROCESSING UNIT

Central processing unit is the heart of the computer; this is the component that actually executes instructions. In addition to these components, many others make it possible for the basic components to work together efficiently.

For example, every computer requires a bus that transmits data from one part of the computer to another. This is usually a single microprocessor chip, although its subsystems can be on more than one chip. The CPU at least includes a control unit, timing circuitry, an arithmetic logic unit (ALU) and also usually contains registers for temporary storage.
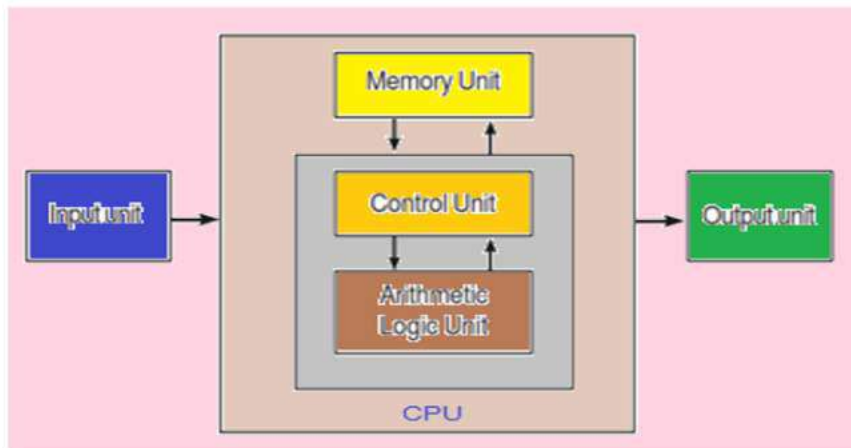
Figure 6.1

CONTROL UNIT (CU)

The control unit directs the operation of the computer, managing the interaction between subunits and processes input and output signal and also storage is performed under the supervision of this unit. It takes instructions from the memory and executes them, performing tasks such as accessing data in memory, calling on the ALU or performing Control Unit. It decides when to start receiving data, when to stop it, where to store data, etc. It takes care of step-by-step processing of all operations inside the computer. Input / Output. Control is one of the most difficult parts to design; thus it is the most likely source of bugs in designing an original architecture. Microprocessors consist of both hard wired control and micro programmed control. In both cases, the designer determines a sequence of states through which the computer cycles, each with inputs to examine and outputs to activate other CPU subsystems (including activating itself, indicating which state to do next).

For example, the sequence usually starts with "Fetch the next instruction from memory," with control outputs to activate memory for a read, a program counter to send the address to be fetched and an instruction register to receive the memory contents. Hard wired control is completely via circuitry, usually with a programmed logic array. Micro programmed control uses a microprocessor with a modifiable control memory, containing micro code or micro instructions. An advantage of micro programmed control is flexibility: the code can be changed without changing the hardware, making it easier to correct design errors.

A device that controls the transfer of data from a computer to a peripheral device and vice versa. For example, disk drives, display screens, keyboards and printers all require controllers. In personal computers, the controllers are often single chips. When you purchase a computer, it comes with all the necessary controllers for standard components, such as the display screen, keyboard, and disk drives. If you attach additional devices, however, you may need to insert new controllers that come on expansion boards. Controllers must be designed to communicate with the computer's expansion bus. There are three standard bus architectures for PCs - the AT bus, PCI (Peripheral Component Interconnect) and SCSI. PCI is a 64-bit bus, though it is usually implemented as a 32 bit bus. It can run at clock speeds of 33 or 66 MHz. At 32 bits and 33 MHz, it yields a throughput rate of 133 MBps. SCSI interfaces provide for faster data transmission rates (up to 80 megabytes per second) than standard serial and parallel ports. In addition, you can attach many devices to a single SCSI

port, so that SCSI is really an I/O bus rather than simply an interface. Although SCSI is an ANSI standard, there are many variations of it, so two SCSI interfaces may be incompatible. For example, SCSI supports several types of connectors. While SCSI has been the standard interface for Macintoshes, the iMac comes with IDE, a less expensive interface, in which the controller is integrated into the disk or CD-ROM drive. The following varieties of SCSI are currently implemented:

ARITHMETIC LOGIC UNIT

The arithmetic logic unit (ALU) performs logical operations such as AND, OR and SHIFT and arithmetic operations such as addition, subtraction, multiplication and division. The ALU depends on the control unit to tell it which operation to perform and also to trigger other devices (memory, registers and I/O) to supply its input data and to send out its results to the appropriate place. The ALU often only performs simple operations. Complex operations, such as multiplication, division and operations involving decimal numbers are performed by dedicated hardware, called floating-point processors, or floating point units. These may be included on the original mother board or may be optional upgrades. Nowadays in modern microprocessors, usually a floating point unit is integrated on the same microprocessor IC.

DATA BUSES

There are three buses, the address bus, the data bus and the control bus. The memory consists of a number of locations, each individually identified by an address. The address bus is therefore used to specify the memory location or input / output port involved in the transfer. It is a one way bus and may have anything from 4 to 64 lines depending on the number of memory addresses there are, 8 lines give $2^8 = 256$ addresses. The data bus is a bi-directional bus and is used to carry the data being transferred to and from the memory or input and output transfer. The control bus comprises input and output lines which synchronize the microprocessor's operation with that of the external circuitry i.e. read/write controls, timing signals, input/output selection. This is also a bi-directional bus.(Figure 6.2)
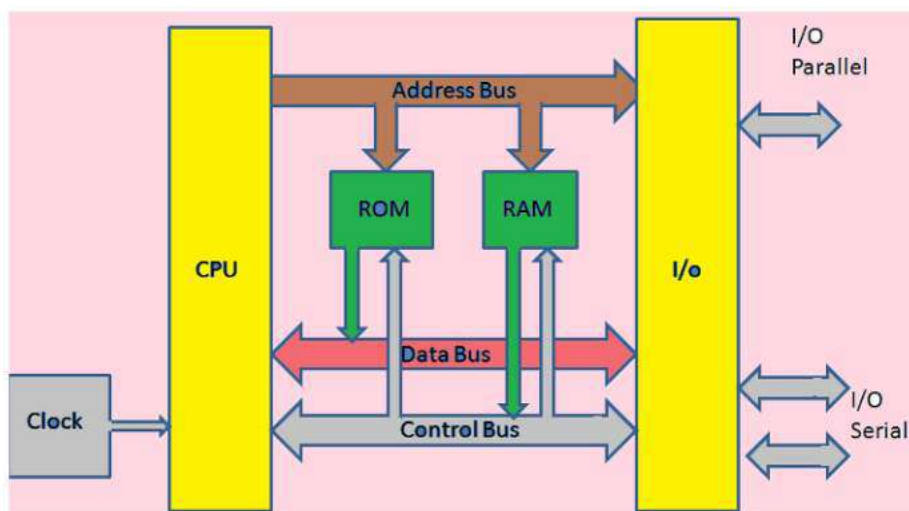

Figure 6.2: Block diagram of Micro Computer

Computers and other digital circuits rely on stored information, either data to be acted upon or instructions to direct circuit actions. This information is stored in memory devices, in binary form. This section first discusses how to access an individual item in memory and then compares different memory types, which can vary how quickly and easily an item is accessed.

MEMORY TYPES

The concepts described above are applied to several types of random-access, semiconductor memory. Semiconductor memories are categorized by the ease and speed with which they can be accessed and their ability to "remember" in the absence of power.

VOLATILE MEMORY

Sequential-access memory (SAM) must be accessed by stepping past each memory location until the desired location is reached. Magnetic tapes implement SAM; to reach information in the middle of the tape, the tape head must pass over all of the information on the beginning of the tape. Two special types of SAM are the queue and the push-down stack. In a queue, also called a first-in, first-out (FIFO) memory, locations must be read in the order that they were written.

The queue is a "first-come, first-served" device, like a line at a ticket window. The push-down stack is also called last-in, first-out (LIFO) memory. In LIFO memory, the location written most recently is the next location read. LIFO can be visualized as a stack, always adding to and removing from the "top" of the stack. Random-access memory (RAM) allows any memory cell to be accessed at any instant, with no time wasted stepping past the "beginning" parts of the data. Random-access memory is like a bookcase; any book can be pulled out at any time. It is usually faster to access a desired word in RAM than in SAM. Also, all words in RAM have the same access time, while each word in a SAM has a different access Time based on its position. Generally, the semiconductor memory devices internal to computers are random-access memories. Magnetic devices, such as tapes and disks, have at least some sequential access characteristics. We will leave tapes and disks for a later section and concentrate here on random-access, solid-state memories. Most RAM chips are volatile, meaning that stored information is lost if power is removed. RAM is either static or dynamic. Dynamic RAM (DRAM) stores a bit of information as the presence or absence of charge. This charge, since it is stored in a capacitor, slowly leaks away. It must be refreshed periodically. Memory refresh typically occurs every few milliseconds and is usually performed by a dynamic RAM controller chip. Static RAM (SRAM) stores a bit of information in a flip-flop. Since the bit will retain its value until Sequential-access memory (SAM) must be accessed by stepping past each memory location until the desired location is reached. Magnetic tapes implement SAM; to reach information in the middle of the tape, the tape head must pass over all of the information on the beginning of the tape. Two special types of SAM are the queue and the push-down stack. In a queue, also called a first-in, first-out (FIFO) memory, locations must be read in the order that they were written.

choice since the data can be written after manufacture. A PROM is manufactured with all its diodes or transistors connected.

This type of PROM can be written only once. EPROM, EEPROM Two types of PROMs that can be "erased" and reprogrammed are EPROM's and EEPROM's. The transistors in UV erasable PROMs (EPROM's) have a floating gate surrounded by an insulating material. When programming with a bit value, a high voltage creates a negative charge on the floating gate. Exposure to ultraviolet light erases the negative charge.

Similarly, electrically erasable PROMs (EEPROM's) erase their floating-gate values by applying a voltage of the opposite polarity ROM's are practical only for storing data or programs that do not change frequently and must survive when power is removed from the memory. The programs that start up a computer when it is first switched on or the memory that holds the call sign in a repeater are prime candidates for ROM. Flash also known as FEPROM is one of the newest types of non-volatile memory. In this device data is erased and reprogrammed in blocks, unlike the byte by byte altering capability of EEPROM. FLASH memory has the density of EPROM's and the electrical erase capability of standard EEPROM's. FLASH is used in digital cameras to store pictures; PC's store their BIOS on FLASH memory chips, and MP3 audio recorders use FLASH to store music. For some situations, the ideal memory would be as non-volatile as ROM but as easy to write to as RAM. The primary example is data that must not be allowed to perish despite a power failure. Low-power RAMs can be used in such applications.

DATA STORAGE

All computers work on a binary numbering system, i.e. they process data in one's or zero's. This 1 or 0 level of storage is called a bit. A byte consists of eight bits and one nibble consist of four bits. A kilobyte (KB) consists of 1024 bytes. A Megabyte (MB) consists of 1024 kilobytes. A gigabyte (GB) consists of 1024 megabytes. But usually we use to express the amount of storage provided by a memory device is in kilobytes (Kbyte). It is important to note that a kilobyte of memory is actually 1024 bytes (not 1000 bytes). The reason for choosing the Kbyte rather than the Kbyte (1000 bytes) is that 1024 happens to be the nearest power of 2(note that $2^{10} = 1024$).

PERIPHERAL DEVICES

Peripheral devices are connected to the computer externally. These devices are used for performing some specific functions. Peripheral devices are as follows:

1. Input Devices
2. Output Devices
3. Other Peripheral

DIFFERENCE BETWEEN MICROCONTROLLER AND MICROPROCESSOR

MICRO CONTROLLER
- It is a single chip
- Consists Memory, I/o ports

MICRO PROCESSER
- It is a CPU
- Memory, I/O Ports to be connected externally

CP

MEMORY

I/O PORTS

CPU ↔ MEMORY

I/O PORTS
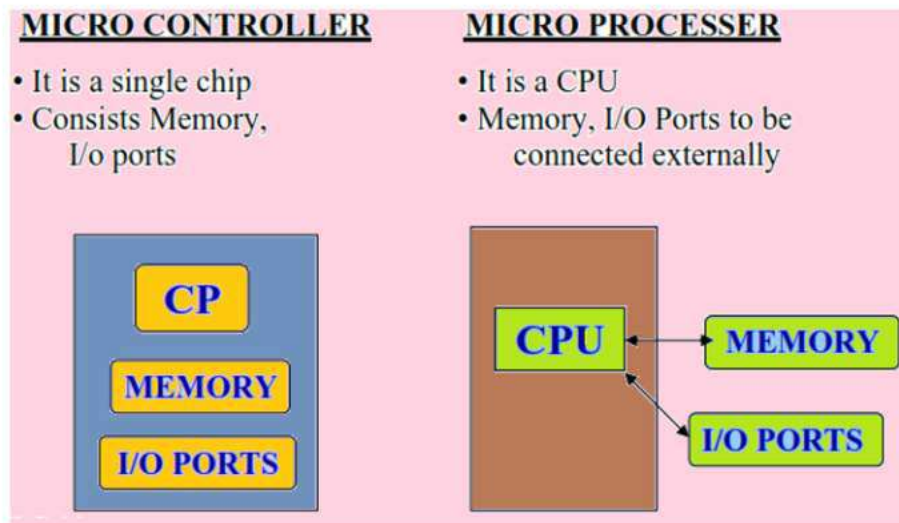
Figure 6.3

HARDWARE/DATA STORAGE DEVICES

The term hardware refers to the physical components of your computer such as all the Input and Output devices, Storage devices such as hard disk, floppy disk, CD-ROM disks, DVD drives. Magnetic media are essential input/output devices since they provide additional memory. The earliest ways to store programs and data were on punched cards and tape. Some early home computers used audio cassettes. Disk storage is prevalent when random access is needed. In some ways, disk storage is similar to that of a record player. The data is stored in circles (tracks) on a round platter (disk or diskette) and accessed by a device (a head) moving over the platter. Unlike the record player, the tracks are concentric rather than spiral and the head can write as well as read. Usually the tracks are divided into equal-sized storage units, called sectors. Also, since the disk has two sides, most disks can store information on both sides.

Therefore, locating a piece of information in disk memory means identifying three coordinates: the side, track and sector. Accessing a piece of information on the disk system involves a number of wait times until the data access is complete head is attached to a movable arm, so there is a seek time for the movable arm to position the read/write head on the appropriate track. In a fixed system, each track has its own read/write head, so seek time is zero since the head is immediately in position. Second, the data must rotate into position under the read/write head. This time is called latency. Finally, there is the normal time for the read/write to occur.

A number of types of disk technology are available. In hard disk systems, the disk is rigid and the read/write head does not contact the disk directly. The absence of friction between the head and disk allows finer head positioning and higher disk speeds. Thus, hard disks hold more data and are accessed more quickly than floppy disks. Floppy disks enclose the magnetic-media platter in a casing, as shown in Figure-6.4, so the disk can be carried around. The floppy disk can be inserted into a disk drive and the read/write head automatically extended; when done, the read/write head is automatically retracted before the disk is ejected from the drive. Variations in floppy disks include

single-sided (SS) or double-sided (DS); single, double or high density; and 3 1 /2. The density refers to the disk format used by the disk controller. High data density allows more data to be written to the disk but requires a higher quality diskette. Not all disks can e written as high density and not all disk drives can read high density disks. Dust and dirt on the disk and the imperfections in the disk surface gradually damage both the disk and the head. This means that disks eventually wear out, and the data on the disk will probably be lost. Therefore, it is prudent to make backup copies of your disks, stored in a clean, dry, cool place.

CD-ROM is an abbreviation of Compact Disc Read-Only Memory, a type of computer memory in the form of a compact disc that is read by optical means. A CD- ROM drive uses a low- power laser beam to read digitized (binary) data that has been encoded in the form of tiny pits on an optical disk. The drive then feeds the data to a computer for processing. The standard compact disc was introduced in 1982 for digital audio reproduction. But, because any type of information can be represented digitally, the standard CD was adapted by the computer industry, beginning in the mid-1980s, as a low-cost storage-and-distribution medium for large computer programs, graphics, and databases. With a storage capacity of 680 megabytes, the CD-ROM found rapid commercial acceptance as an alternative to so-called floppy disks (with a maximum capacity of 1.4 megabytes). Unlike conventional magnetic storage technologies (e.g., tapes, floppy disks, and hard disks), CD's and CD-ROM's are not recordable--hence the tag "read only." This limitation spurred the development of various recordable magnetic-optical hybrid storage devices; but they generally failed to penetrate beyond the publishing world, where large multimedia files are regularly exchanged, because of incompatibility with standard CD and CD-ROM players. In the early 1990s a new type of CD became available: CD-Recordable, or CD-R.

| Floppy Disk | Hard disk | DVD Drives | CD-ROM Disc |

Figure 6.4

STORAGE

These discs differ from regular CD's in having a light-sensitive organic dye layer which can be "burned" to produce a chemical "dark" spot, analogous to an ordinary CD's pits, that can be read by existing CD and CD-ROM players. Such CD's are also known as WORM discs, for "Write Once Read Many." A rewritable version based on excitable crystals and known as CD-RW was introduced in the mid-1990s. Because both CD-R and CDRW recorders originally required a computer to operate, they had limited acceptance outside of use as computer software and data backup devices. To handle the proliferation of ever-larger multimedia files (audio, graphic, and video) in computer games, educational software, and electronic encyclopedia as CD-ROM well as high-definition movies for television entertainment systems an expanded storage medium, digital versatile disc (DVD), was introduced in 1995. In 1995 Philips and Sony introduced a new type of

disc, known as a digital versatile disc (DVD), which was able to store up to 4.7 gigabytes of data, such as high-definition digital video files. A DVD has the same dimensions as a standard CD but cannot be read by a standard CD player, although a DVD player can read standard CD's. DVD players use a higher-power red laser (0.65 micrometre) that enables smaller pits (0.4 micrometre) and separation tracks (0.74 micrometre) to be used.

Magnetic Tape is one of the more inexpensive options for auxiliary memory. Tape access time is slow, since the data must be accessed sequentially, so tape is primarily used for backup copies of a system's memory. Tape is available in cassette form (common sizes are comparable to the cassettes for a portable tape player and VCR tapes) and on reels (diameter is approximately one foot). Digital audio tape (DAT) is replacing other forms of tape backup system in newer computer systems. A single 4-mm- wide DAT cartridge, which fits in the palm of your hand, can hold over 2 gigabytes (GB) of data (1 GB = 1024 MB).

SOFTWARE

In order to perform any task, you have to give a set of instructions in a particular sequence to the computer. These sets of instructions are called Programs. Software refers to a set of programs that makes the hardware perform a particular set of tasks in particular order.
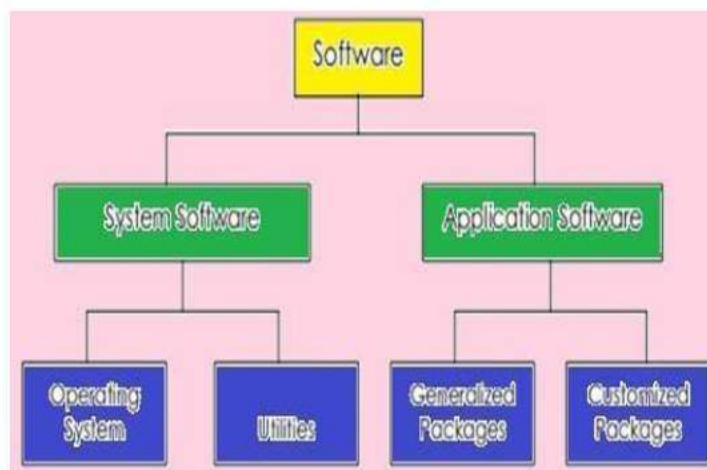
Figure 6.5: Classification of Software

System Software

When you switch on the computer the programs stored in ROM are executed which activates different units of your computer and makes it ready for you to work on it. This set of programs can be called system software.

a. OPERATING SYSTEM

An Operating system is system software that provides an interface for a user to communicate with the computer, manages hardware devices (disk drives, keyboard, monitor, etc), manages and maintains disk file systems and supports application programs.

These are programs that bridge the gap between the functionality of an OS and the needs of users Utility programs are a broad category of software such as compress (zip)/uncompress (unzip) files software, antivirus software, split and join files software, etc.

Application Software

Application software is a set of programs, which are written to perform specific tasks, for example: An application package for managing library known as library information system is used to manage information of library such as: keeping book details, account holder details, book issue details, book return details etc.

1. GENERALIZED PACKAGES

These are user friendly software's written to cater to user's very general needs such as preparing documents, drawing pictures, database to manage data/information, preparing presentations etc. These are Word Perfect, MS-Word, Lotus Smart suites, MS Excel, Presentation Graphics, MS-PowerPoint, Paint shop pro, Adobe Photoshop.

2. CUSTOMIZED PACKAGES

These are the applications that are customized (or developed) to meet the specific requirements of an organization/institution. For Example: Student information details, Payroll packages, inventory control etc. These packages are developed using high-level computer language.

Computer Languages

Languages are a means of communication. Communication with computers is carried out through a language. This language is understood both by user and the machine. Just as every language like English, Hindi has its every computer language is bound by rules known as SYNTAX of that language. The user is bound by that syntax while communicating with the computer system. Computer languages are broadly classified as:

1. LOW LEVEL LANGUAGE
The term low level means closeness to the way in which machine understand. The low level languages are:

(a) MACHINE LANGUAGE

This is the language (in the form of 0's and 1's, called binary numbers) understood directly by the computer. It is machine dependent. It is difficult to learn and even more difficult to write programs.

(b) ASSEMBLY LANGUAGE

This is the language where the machine codes comprising of 0's and 1's are substituted by symbolic codes (called mnemonics) to improve their understanding. It is the first step to improve programming structure. Assembly language programming is simpler and less time consuming than machine level programming, it is easier to locate and correct errors in assembly language than in machine language programs.

2. HIGH LEVEL LANGUAGE

This language has been evolved which uses normal English like, easy to understand statements to solve any problem. Higher level languages are computer independent and programming becomes quite easy and simple. These are BASIC (Beginners All Purpose Symbolic Instruction Code), COBOL (Common Business Oriented language), FORTRAN (Formula Translation), C, C++.

COMPILER

The software (set of programs) that reads a program written in high level language and translates it into an equivalent program in machine language.

Source Program (Higher Level Language) → Compiler → Object Program (Machine Language)

Figure 6.5 : Compiler

ASSEMBLER

The program written by the programmer in high level language is called source program and the program generated by the compiler after translations called as object program. The software (set of programs) that reads a program written in assembly language and translates it into an equivalent program in machine language is called as Assembler.
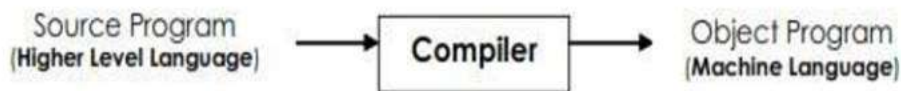
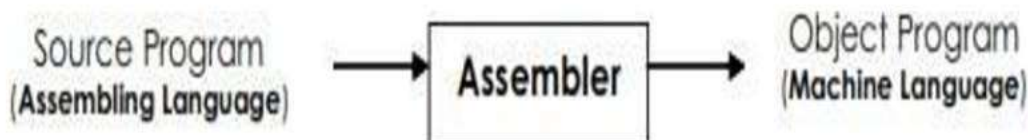Source Program (Assembling Language) → Assembler → Object Program (Machine Language)

Figure 6.6: Assembler

A day, Modern aircraft use increasingly sophisticated avionic systems which involve the use of microprocessor based computer systems. These systems combine hardware and software and are capable of processing large amounts of data in a very small time. In an old type of Digital Flight Data Recorder, airplane operating parameters with relation to time are recorded for later use during performance evaluation or during accident investigation. This recorder has a write- and a erase head and stores the last actual flight parameters The old Quick Access Recorder (QAR), or also known as Performance Maintenance Recorder (PMR) uses a 'Tape Low' Indicators on it. Recording of parameters begins on track one of the tape. At the end of the track (starting with one), the recorder senses the end-of-tape, changes direction and records on the next track in the opposite direction and so on, until the sensing end-of-tape is detected. Because this recorder type has only a write head, the cassette has to be changed before reaching the end of tape.

In a microprocessor system the functions of the CPU are provided by a single very large scale integrated (VLSI) microprocessor chip. This chip is equivalent to many thousands of individual transistors. Semiconductor devices are also used to provide the read/write and read-only memory. Strictly speaking, both types of memory permit 'random access' sinceretrieved with equal ease regardless of its actual location within the memory. Despite this, the term 'RAM' has become synonymous with semiconductor read/write memory.

The basic components of the system (CPU, RAM, ROM and I/O) are linked together using a multiple wire connecting system know as a bus. There are three different types of buses, the address bus used to specify memory locations; the data bus on which data is transferred between devices; and the control bus which provides

Timing and control signals throughout the system. The number of individual lines present within the address bus and data bus depends upon the particular microprocessor employed. Signals on all lines, no matter whether they are used for address, data, or control, can exist in only two basic states: logic 0 (low) or logic (high). Data and addresses are represented by binary numbers (a sequence of 1s and 0s) that appear respectively on the data and address bus. Some basic microprocessors designed for control and instrumentation applications have an 8-bit data bus and a 16-bit address bus. More sophisticated processors can operate with as many as 64 or 128 bits at a time.

The largest binary number that can appear on an8-bit data bus corresponds to the condition when all eight lines are at logic 1. Therefore the largest value of data that can be present on the bus at any instant of time is equivalent to the binary number 11111111 (or 255). Similarly, most the highest address that can appear on a 16-bit address bus is 1111111111111111 (or 65,535). The full range of data values and addresses for a simple microprocessor.

Finally, a locally generated clock signal provides a time reference for controlling the transfer of synchronous data within the system. The clock signal usually consists of a high-frequency square wave pulse train derived from an accurate quartz crystal controlled oscillator.

REFERENCE COMPUTER

Although computers can be classified by hardware as analog, digital, or hybrid, they are more often classified by their tasks or application. A computer which may be used for a source of information or data can be called a reference computer. Reference signals from this computer may be self-contained and only provides outputs. An Inertial Reference System (IRS) is one example of a reference computer. This system is a laser gyro and accelerometer based reference system used to generate such outputs as airplane attitude, heading, acceleration and angular information. Other than for initialization purposes, the IRS needs no inputs to perform its task. Some of the units utilizing this information as a reference are the Flight Control Computers, the pilot's Horizontal Situation indicators, and the Flight Management Computer.
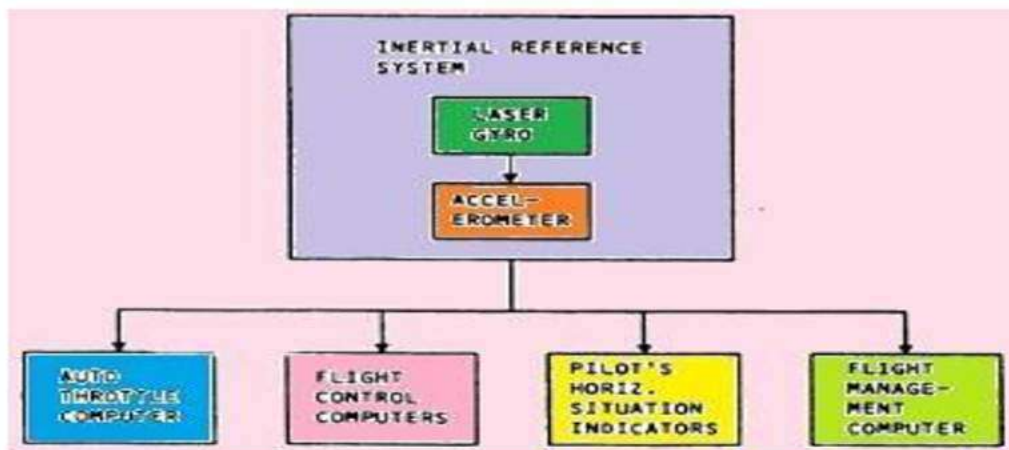
Figure 6.7

INFORMATIONAL, WARNING & DISPLAY COMPUTERS

A computer system that collects data from various places, processes it, and formats it for display and warning can be called an electronic Instrument System (Airbus) or an Engine Indication and Crew Alerting System (Boeing). The main task of such a computer system is to collect data and display it in a central place. During the different phases of a flight, from power up through touchdown, the flight crew is often in need of information concerning a certain airplane system. Information needed may include for example total air temperature, engine oil levels, hydraulic pressures, and engine vibration levels. On the ground, the maintenance personnel often need to recall certain events that occurred during the flight, such as out of normal parameters on an engine (over speed), or Auxiliary Power Unit voltage information. The flight crew has various types of information available to them before, during and after a flight.
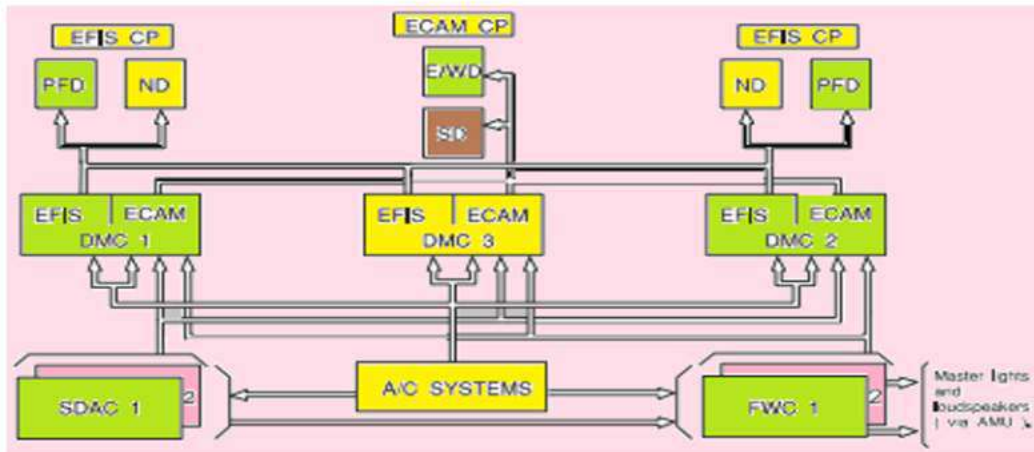
Figure 6.8 Airbus EIS

Parameters used to set and monitor engine thrust are displayed on a cathode ray tube (CRT) full time and the remaining engine parameters may be selected for display by the crew. Maintenance information can be displayed when required by maintenance personnel. Airplane configuration, equipment cooling and status, electrical/ hydraulic parameters, performance data and engine exceedance are some of the types of maintenance information available. On Figure 6.8 the Airbus Electronic Instrument System is shown. It is divided in an Electronic Flight Instrument System EFIS, and an Electronic Centralized Aircraft Monitoring ECAM. The EFIS provides flight information and the ECAM provides system and warning information. The Electronic Instrument System comprises seven computers:

- Three identical Display Management Computers (DMC's)
- Two identical Flight Warning Computers (FWC's)
- Two identical System Data Acquisition Concentrators (SDAC's).

The DMC's comprise two independent parts: one for the EFIS function and one for the ECAM function.

CONTROLLING COMPUTERS

A computer with the primary task of controlling something can be called a controlling computer or controller. This is one of the largest categories of computers. In industry today nearly anything that can be controlled by a computer. Computerized controllers range from simple temperature controllers to entire systems for controlling a complete factory. Airplanes have a variety of systems, surfaces, and devices needing control during operation, both in the air and on the ground It is impractical to have the flight crew manually control all of the necessary systems, so computers are used to lighten the crew's workload by providing automatic control. An example would be the control of the slats and the flaps on an Airbus A330:

- The Slat Flap Control Computer (SFCC) provides a means to monitor the slat and flap lever position and to control the slat and flap position on the wings.

- Position of the surfaces is selected from a control lever which transmits the demand to the Slat Flap Control Computers through a Command Sensor Unit.

- The SFCC's, which are identical, ensure the control and monitoring of the slat and flap system. On lever demand, the SFCC's send signals to a Power Control Units to energize the valve blocks.

- Two hydraulic motors in each Power Control Unit provide hydraulic actuation. Each of them is powered by a different hydraulic system and has its own valve block and pressure off brake. The valve blocks control the direction of rotation and the speed of their related PCU output shaft. The hydraulic motors move the transmission through a differential gearbox. Then torque shafts and gearboxes transmit the mechanical power to the actuators which drive the surfaces. Wing tip brakes are provided in order to stop and lock the system when certain types of failure are detected. Feedback signals sent by dedicated Position Pick-off Units are used by the computers to control and monitor the system. A Feedback PPU provides signals concerning the PCU output shaft position, while two Asymmetry PPU's send information about surface actual position. In addition signals sent from an Instrumentation PPU are used for position indicating on the ECAM.
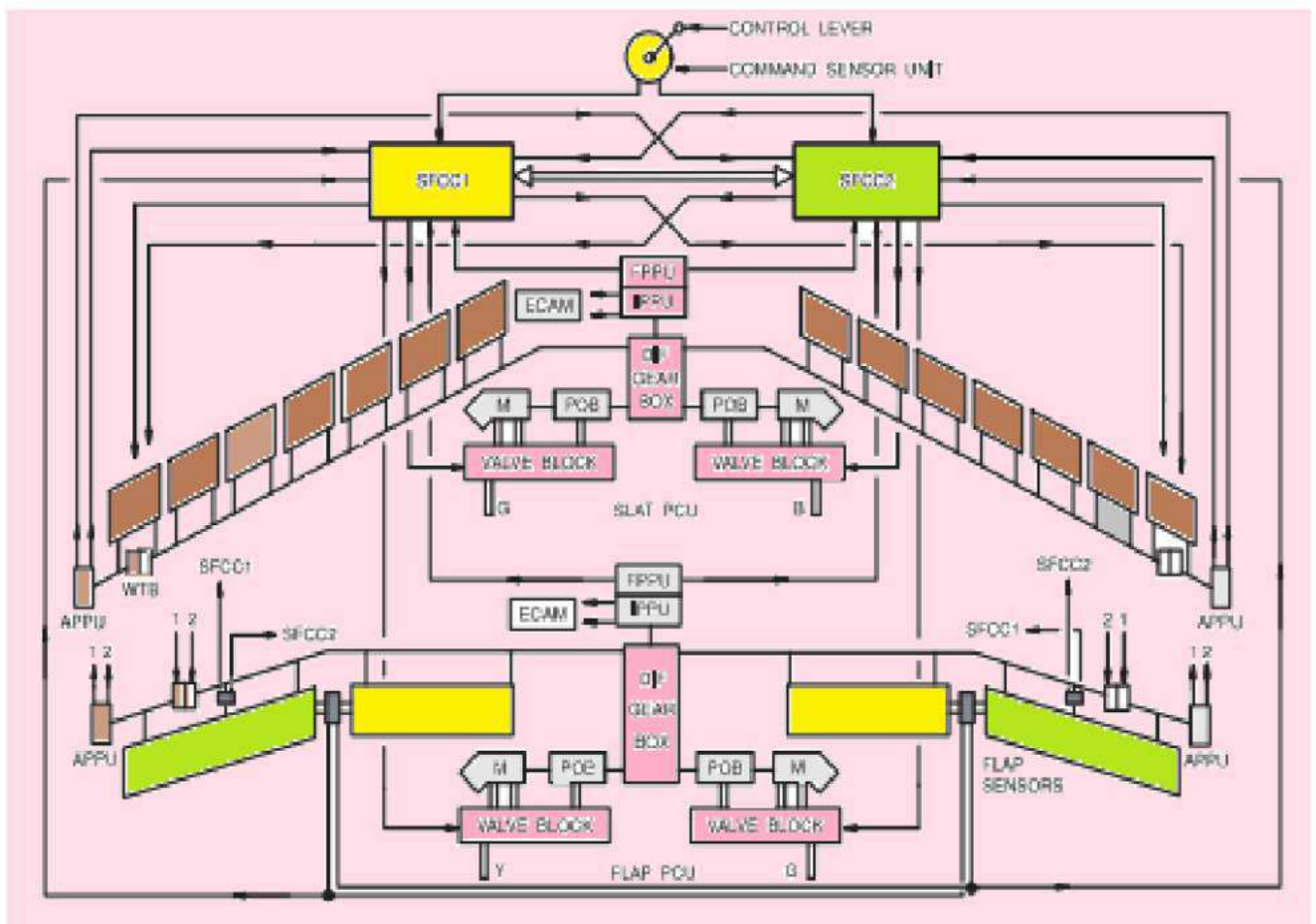

Figure 6.9: Flap Slat Controlling System.

5.7 MICROPROCESSORS

Microprocessor is a computer Central Processing Unit (CPU) on a single integrated circuit (IC), or at most a few integrated circuits and it is the controlling element in a computer. The microprocessor central processing unit (CPU) forms the heart of any microprocessor or microcomputer system computer and, consequently, its operation is crucial to the entire system. The primary function of the microprocessor is that of fetching, decoding, and executing instructions resident in memory. As such, it must be able to transfer data from external memory into its own internal registers and vice versa. All modern CPUs are microprocessors making the micro- prefix redundant. The microprocessor is a multipurpose; It is an example of sequential digital logic, as it has internal memory. Microprocessors operate on numbers and symbols represented in the binary numeral system. It contains millions of transistors connected by wires. The microprocessor is:

1. A programmable device that accepts digital data as input, processes it according to instructions stored in its memory, and provides results as output. Registers are used for temporary storage of addresses and data;
2. Transfer Data between itself and the memory or I/O system,
3. Capable of performing arithmetic and logical operations with the help of an arithmetic logic unit (ALU).

The integration of a whole CPU onto a single chip or on a few chips greatly reduced the cost of processing power. The integrated circuit processor was produced in large numbers by highly automated processes, so unit cost was low. Single-chip processors increase reliability as there are many fewer electrical connections to fail. As microprocessor designs get faster, the cost of manufacturing a chip (with smaller components built on a semiconductor chip the same size) generally stays the same.

Before microprocessors, small computers had been implemented using racks of circuit boards with many medium- and small- scale integrated circuits. Microprocessors integrated this into one or a few large-scale ICs. Continued increases in microprocessor capacity have since rendered other forms of computers almost completely obsolete with one or more microprocessors used in everything from the smallest embedded systems and handheld devices to the largest mainframes and supercomputers. It has different parts, a unit that receives and decodes instructions and a means of controlling and timing operations within the system.

Figure 7.1 shows the principal internal features of a typical 8-bit microprocessor as well as the data paths that link them together. Because this diagram is a little complex, we will briefly explain each of these features and what they do.

(a) ACCUMULATOR

The accumulator functions both as a source and as a destination register for many of the basic microprocessor operations. As a source register it contains the data that will be used in a particular operation whilst as a destination register it will be used to hold the result of a particular operation. The accumulator (or A register) features in a very large number of microprocessor operations, consequently more reference is made to this register than any others.

(b) INSTRUCTION REGISTER

The instruction register provides a temporary storage location in which the current microprocessor instruction is held whilst it is being decoded. Program instructions are passed into the microprocessor, one at time, through the data bus. On the first part of each machine cycle, the instruction is fetched and decoded. The instruction is executed on the second (and subsequent) machine cycles. Each machine cycle takes a finite time (usually less than a microsecond) depending upon the frequency of the microprocessor's clock.

(c) DATA BUS (D 0 to D 7)

The external data bus provides a highway for data that links all of the system components (such as random access memory, read- only memory, and input/output devices) together. In an 8-bit system, the data bus has eight data lines, labelled D 0 (the least significant bit) to D 7 (the most significant bit) and data is moved around in groups of eight bits, or bytes. With a sixteen bit data bus the data lines are labelled D 0 to D 15, and so on.

(d) DATA BUS BUFFER

The data bus buffer is a temporary register through which bytes of data pass on their way into, and out of, the microprocessor. The buffer is thus referred to as bi-directional with data passing out of the microprocessor on a write operation and into the processor during a read operation. The direction of data transfer is determined by the control unit as it responds to each individual program instruction.

(e) INTERNAL DATA BUS

The internal data bus is a high-speed data highway that links all of the microprocessor's internal elements together. Data is constantly flowing backwards and forwards along the internal data bus lines.

(f) GENERAL PURPOSE REGISTERS

Many microprocessor operations (for example, adding two 8-bit numbers together) require the use of more than one register. There is also a requirement for temporarily storing the partial result of an operation whilst other operations take place. Both of these needs can be met by providing a number of general purpose registers. The use to which these registers are put is left mainly up to the programmer.
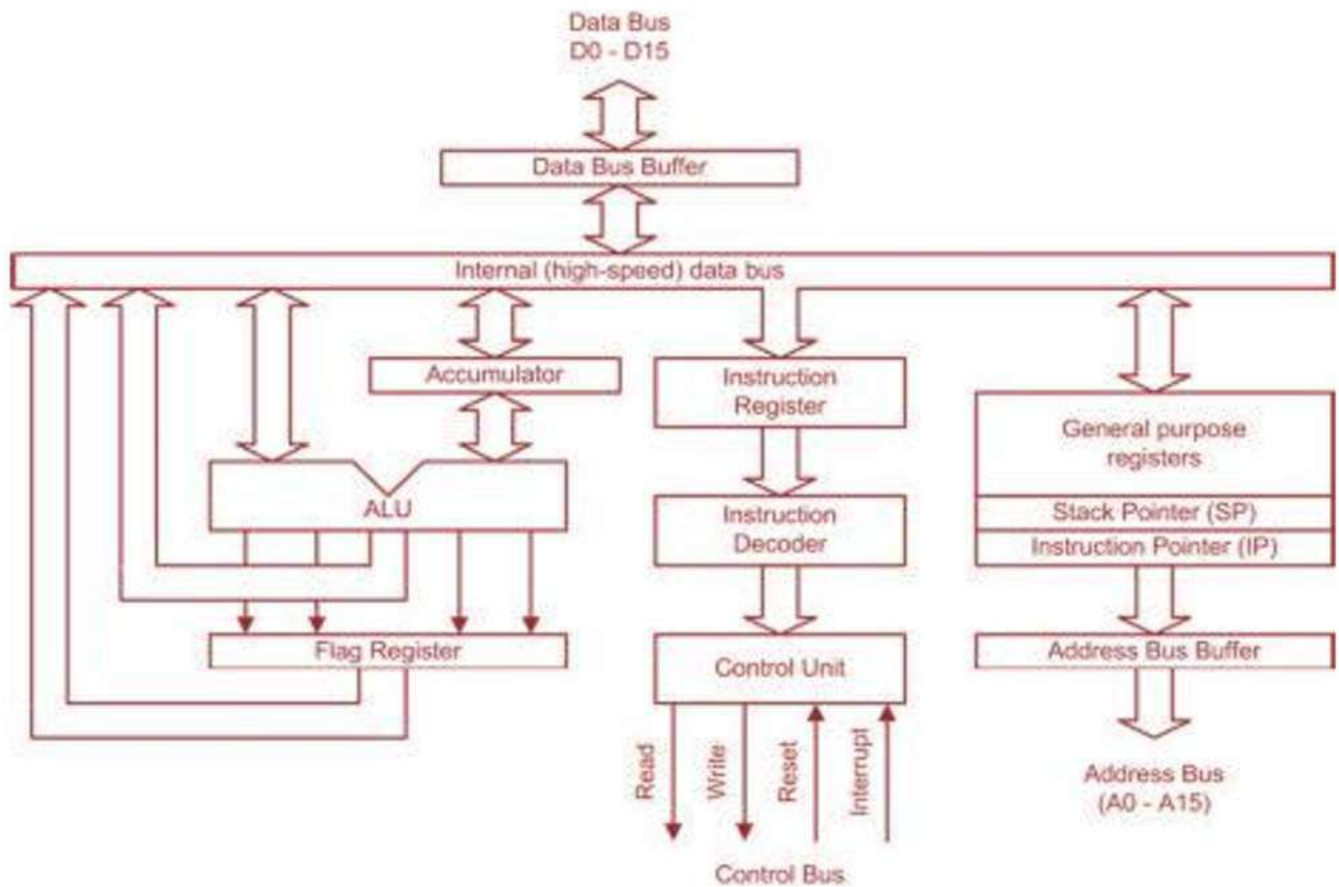
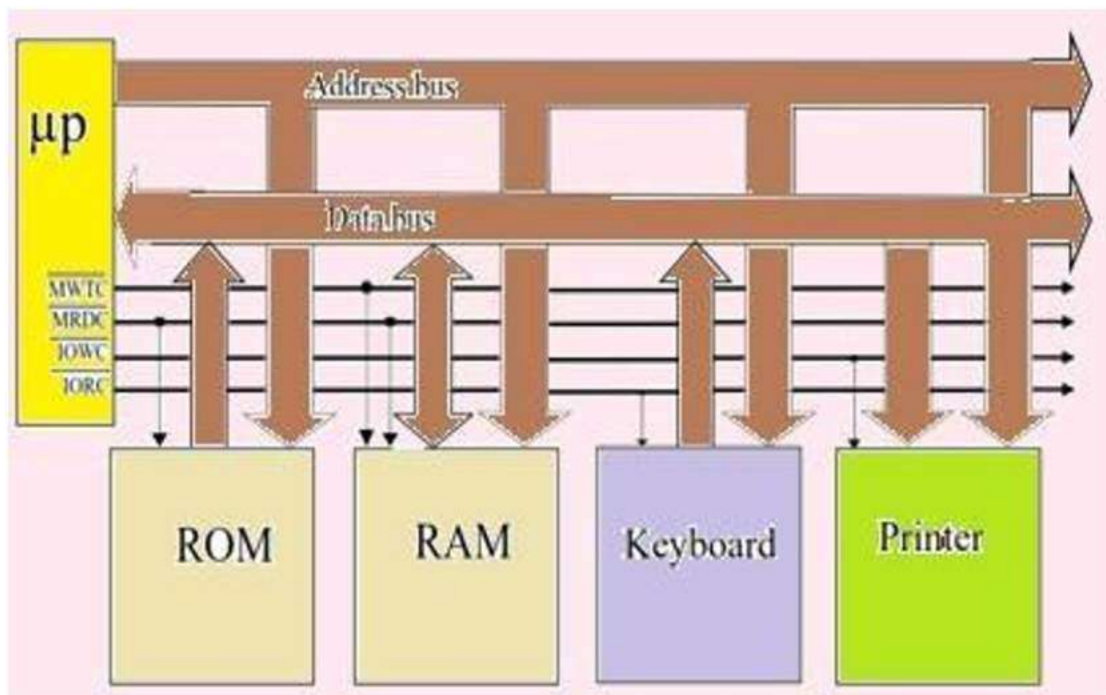Figure 7.1: Internal Architecture of a Basic 8-bit Microprocessor CPU

Figure 7.2: Computer System Showing the Buses Structure

(g) STACK POINTER

When the time comes to suspend a particular task in order to briefly attend to something else, most microprocessors make use of a region of external random access memory (RAM) known as a stack. When the main program is interrupted, the microprocessor temporarily places in the stack the contents of its internal registers together with the address of the next instruction in the main program.

When the interrupt has been attended to, the microprocessor recovers the data that has been stored temporarily in the stack together with the address of the next instruction within the main program. It is thus able to return to the main program exactly where it left off and with all the data preserved in its registers. The stack pointer is simply a register containing the address of the last used stack location.

(h) INSTRUCTION POINTER

Computer programs consist of a sequence of instructions that are executed by the microprocessor. These instructions are stored in external random access memory (RAM) or read-only memory (ROM).Instructions must be fetched and executed by the microprocessor in a strict sequence. By storing the address of the next instruction to be executed, the instruction pointer (or program counter) allows the microprocessor to keep track of where it is within the program. The program counter is automatically incremented when each instruction is executed.

(i) ADDRESS BUS BUFFER

The address bus buffer is a temporary register through which addresses (in this case comprising 16-bits) pass on their way out of the microprocessor. In a simple microprocessor, the address buffer is unidirectional with addresses placed on the address bus during both read and write operations. The address bus lines are labeled A0 to A15, where A0 is the least address bus line and A15 is the most significant address bus line. Note that a 16-bit address bus can be used to communicate with 65,536 individual memory locations. At each location a single byte of data is stored.

(j) CONTROL BUS

The control bus is a collection of signal lines that are both used to control the transfer of data around the system and also to interact with external devices. The control signals used by microprocessors tend to differ with different types, however the following are commonly found:

- READ

An output signal from the CPU that indicates that the current operation is a read operation.

- WRITE

An output signal from the CPU that indicates that the current operation is a write operation

- RESET

A signal that resets the internal registers and initializes the instruction pointer program counter so that the program can be restarted from the beginning.

- **IRQ**

An interrupt request from an external device attempting to gain the attention of the CPU (the request may either be obeyed or ignored according to the state of the microprocessor at the time that the interrupt request is received).

NOTE

NMI- Non-maskable interrupt (i.e. an interrupt signal that cannot be ignored by the microprocessor).

(k) ADDRESS BUS (A 0 to A 15)

The address bus provides a highway for addresses that links with all of the system components (such as random access memory, read-only memory, and input/output devices). In a system with a 16-bit address bus, there are sixteen address lines, labeled A 0 (the least significant bit) to A15 (the most significant bit). In a system with a 32-bit address bus there are 32 address lines, labelled A 0 to A 31, and so on.

NOTE

A buses are a number of wires organized to provide a means of communication among different elements in a microcomputer system. Fig 7.2 shows the buses of 8086 microprocessor, these buses are Address bus, Data bus, Control bus.

(l) INSTRUCTION DECODER

The instruction decoder is nothing more than an arrangement of logic gates that acts on the bits in the instruction register and determines which instruction is currently being referenced. The instruction decoder provides output signals for the microprocessor's control unit.

(m) CONTROL UNIT

The control unit is responsible for organising the orderly flow of data within the microprocessor as well as generating, and responding to, signals on the control bus. The control unit is also responsible for the timing of all data transfers. This process is synchronised using an internal or external clock signal (not shown in Fig. 7.1).

(n) ARITHMETIC LOGIC UNIT (ALU)

As its name suggests, the ALU performs arithmetic and logic operations. The ALU has two inputs (in this case these are both 8- bits wide). One of these inputs is derived from the Accumulator whilst the other is taken from the internal data bus via a temporary register (not shown in Fig. 7.1). The operations provided by the ALU usually include addition, subtraction, logical AND, logical OR, logical exclusive-OR, shift left, shift right, etc. The result of most ALU operations appears in the accumulator.

(o) STATUS REGISTER

The result of an ALU operation is sometimes important in determining what subsequent action takes place. The status register (flag register or condition code register) contains a number of individual bits that are set or reset according to the outcome of an ALU operation. These bits are referred to as flags. The following flags are some typical examples of those provided by most microprocessors:

- ZERO

The zero flag is set when the result of an ALU operation is zero.

- CARRY

The carry flag is set whenever the result of an ALU operation (such as addition) generates a carry bit (in other words, when the result cannot be contained within an 8-bit register).
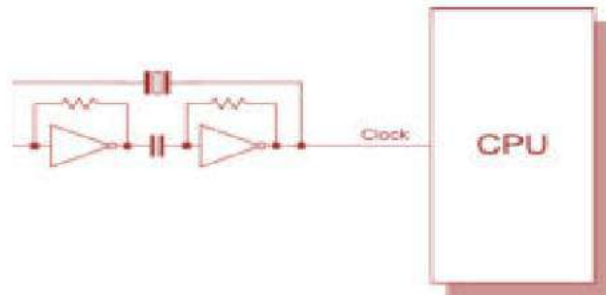
(a)
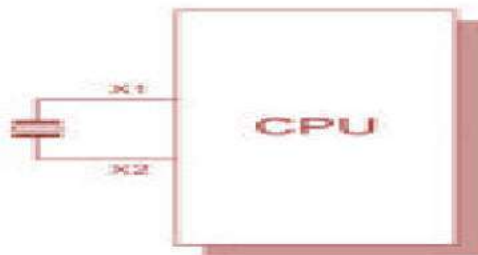
(b)

Figure 7.3
Figure 7.3 : (a) A Typical Microprocessor Clock Circuit. (b) Waveform Produced by the Clock Circuit.

(b)

Figure 7.4: (a) An External CPU Clock. (b) An Internal CPU Clock.

INTERRUPT

The interrupt flag indicates whether external interrupts are currently enabled or disabled

CLOCKS

The clock used in a computer system is simply an accurate and stable square wave generator. In most cases the frequency of the square wave generator is determined by a quartz crystal. A simple 4 MHz square w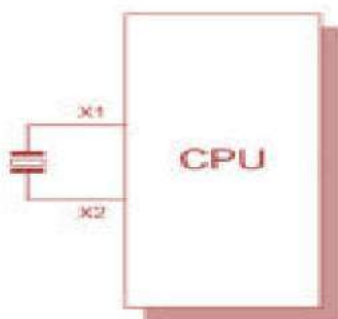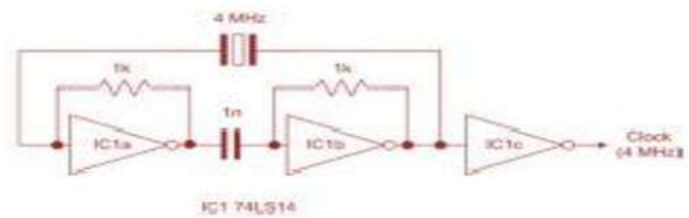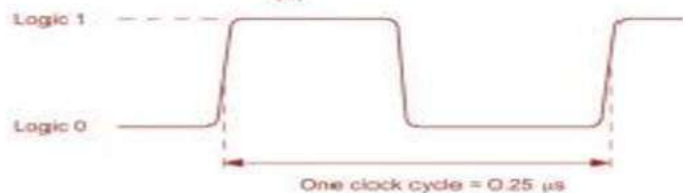ave clock oscillator (together with the clock waveform that is produces) is shown in Figure 7.3. Note that one complete clock cycle is sometimes referred to as a T-state.

Microprocessor central processing units sometimes have an internal clock circuit in which case the quartz crystal (or other resonant device) is connected directly to pins on the microprocessor chip. In Figure 7.4 (a) an external clock is shown connected to a microprocessor whilst in Figure 7.4 (b) an internal clock oscillator is used.

BASIC MICROPROCESSOR ELEMENT OPERATION CONTROL; & PROCESSING UNIT

The majority of operations performed by a microprocessor involve the movement of data. Indeed, the program code (a set of instructions stored in ROM or RAM) must itself be fetched from memory prior to execution. The microprocessor thus performs a continuous sequence of instruction fetch and executes cycles. The act Of fetching an instruction code (or operand or data value) from memory involves a read operation whilst the act of moving data from the microprocessor to a memory location involves a write operation, see Figure 7.5. Each cycle of CPU operation is known as a machine cycle. Program instructions may require several machine cycles (typically between two and five).

The first machine cycle in any cycle consists of an instruction fetch (the instruction code is read from the memory) and it is known as the M1 cycle. Subsequent cycles M2, M3, and so on, depend on the type of instruction that is being executed. This fetch-execute sequence is shown in Figure 7.6. Microprocessors determine the source of data (when it is being read) and the destination of data (when it is being written) by placing a unique address on the address bus. The address at which the data is to be placed (during a write operation) or from which it is to be fetched (during a read operation) can either constitute part of the memory of the system (in which case it may be within ROM or RAM) or it can be considered to be associated with input/output (I/O).

(a)

(b)

Figure 7.5: (a) Read (b) Write Operations

Since the data bus is connected to a number of VLSI devices, an essential requirement of such chips (e.g. ROM or RAM) is that their data outputs should be capable of being isolated from the bus whenever necessary. These chips are fitted with select or enable inputs that are driven by address decoding logic that ensures that external devices (ROM, RAM and I/O) never simultaneously attempt to place data on the bus. The inputs of the address decoding logic are derived from one, or more, of the address bus lines. The address decoder effectively divides the available memory into blocks corresponding to a particular function (ROM, RAM, I/O, etc.). Hence, where the processor is reading and writing to RAM, for example, the address decoding logic will ensure that only the RAM is selected whilst the ROM and I/O remain isolated from the data bus. Within the CPU, data is stored in several registers. Registers themselves can be thought of as a simple pigeon-hole arrangement that can store as many bits as there are holes available. Generally, these devices are can store groups of sixteen or thirty-two bits. Additionally, some registers may be configured as either one register of sixteen bits or two registers of thirty-two bits.

The first machine cycle in any cycle consists of an instruction fetch (the instruction code is read from the memory) and it is known as the M1 cycle. Subsequent cycles M2, M3, and so on, depend on the type of instruction that is being executed. This fetch-execute sequence is shown in Figure 7.6. Microprocessors determine the source of data (when it is being read) and the destination of data (when it is being written) by placing a unique address on the address bus. The address at which the data is to be placed (during a write operation) or from which it is to be fetched (during a read operation) can either constitute part of the memory of the system (in which case it may be within ROM or RAM) or it can be considered to be associated with input/output (I/O).
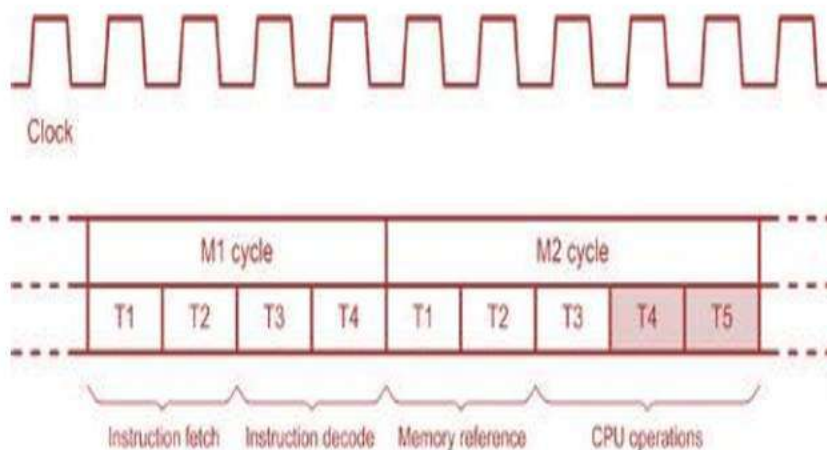

Figure 7.6: A Typical Timing Diagram for a Microprocessor CPUs Fetch-Execute Cycle

Some microprocessor registers are accessible to the programmer whereas others are used by the microprocessor itself. Registers may be classified as either general purpose or dedicated. In the latter case a particular function is associated with the register, such as holding the result of an operation or signaling the result of a comparison. A basic 8-bit microprocessor (the Z80) and its register model is shown in Fig. 7.7.

Note that this microprocessor has six general purpose registers and that these are 8-bits in length. The registers can also be used 'end-on' so that, for example, the BC register pair can be used to hold 16-bit data. Note also, that the Z80's instruction pointer is referred to as the program counter and the status register is called the flag register. Note that different manufacturers use different names for these registers but their function remains the same.

ALU OPERATION

The ALU can perform arithmetic operations (addition and subtraction) and logic (complementation, logical AND, logical OR, etc). The ALU operates on two inputs (eight, sixteen, thirty- two or sixty-four bits in length depending upon the CPU type) and it provides one output (again of eight, sixteen, thirty-two or sixty- four bits depending upon the CPU type). The ALU status is preserved in the flag register so that, for example, an overflow, zero or negative result can be detected and the necessary action can then be taken to deal with this eventuality. A typical example might be that of a program that needs to repeat an operation a set number of times until a zero result is obtained. The control unit is responsible for the movement of data within the CPU and the management of control signals, both internal and external. The control unit asserts the requisite signals to read or write data as appropriate to the current instruction.

Main Register Set	
Accumulator (A)	**Flags (F)**
(B)	(C)
(D)	(E)
(H)	(L)

Special Purpose Registers	
Interrupt Vector (I)	**Memory Refresh (R)**
Index Register (IX)	
Index Register (IY)	
Stack Pointer (SP)	
Program Counter (PC)	
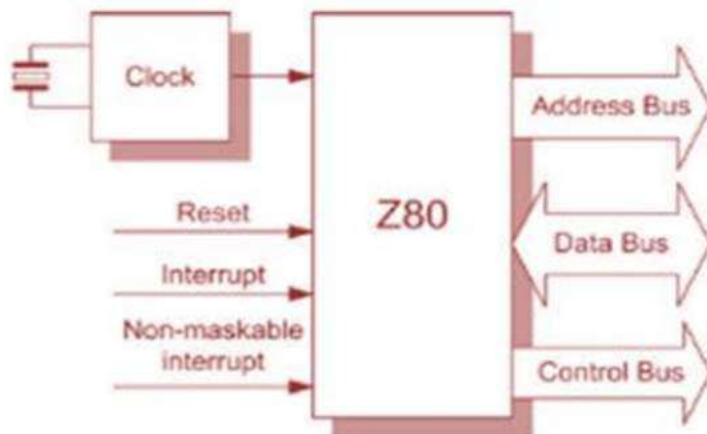
Figure 7.7 : The Z80 CPU (Showing some of its more important control signals and its register modes)

Bit	A Binary digit
Byte	A group of eight bits
Nibble	A group of four bits
ROM	Read Only Memory
Bus	A group of lines that carry the same type of information
RAM	Random Access Memory Or R/WM: Read/Write Memory
Mnemonic	A combination of letters to suggest the operation of an instruction
Program	A set of instructions written in a specific sequence for the computer to accomplish a given task

MICRO ARCHITECTURE OF THE 8086 MICROPROCESSOR

The micro architecture of the 8086 microprocessors employs parallel processing-that is, they are implemented with several simultaneously operating processing units. Figure 7.8 illustrates the internal architecture of the 8086 microprocessors.

They contain two processing units:

1. The Bus Interface Unit (BID) and
2. The Execution Unit (EU).
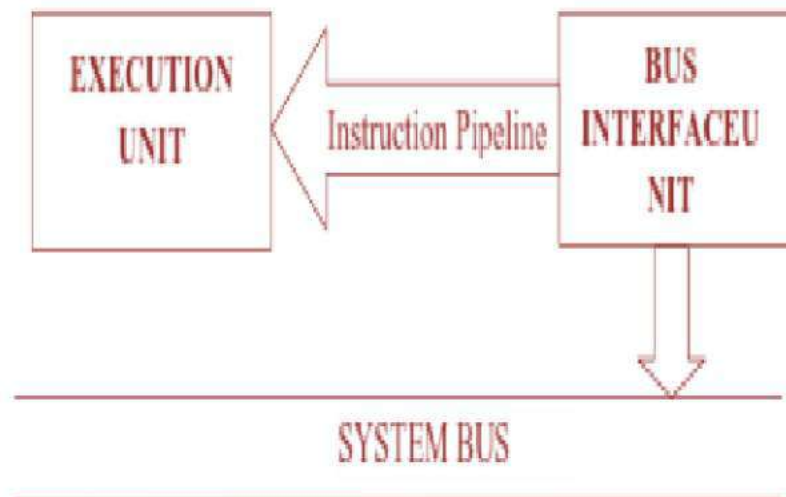
Figure7.8 Micro architecture of the 8086 microprocessors

Each unit has dedicated functions and both operate at the same time. In essence, this parallel processing effectively makes the fetch and execution of instructions independent operations. This results in efficient use of the system bus and higher performance for 8086 microcomputer systems. The BID is free to read the next instruction code when, the queue is not full-that is, it has room for

at least 2 more bytes. The execution unit is not asking it to read or write data from memory. The BID is the 8086's connection to the outside world. By interface, we mean the path by which it connects to external devices.

The BID is responsible for performing all external bus operations, such as instruction fetching, reading and writing of data operands for memory, and inputting or outputting data for input/output peripherals. These information transfers take place over the system bus. The BID is not only responsible for performing bus operations; it also performs other functions related to instruction and data obtained. For instance, it is responsible for instruction queuing and address generation. As shown in Figure 7.9, the BID contains the segment registers, the instruction pointer, the address generation adder, bus control logic, and an instruction queue.

The BID uses a mechanism known as an instruction queue to implement a pipelined architecture.
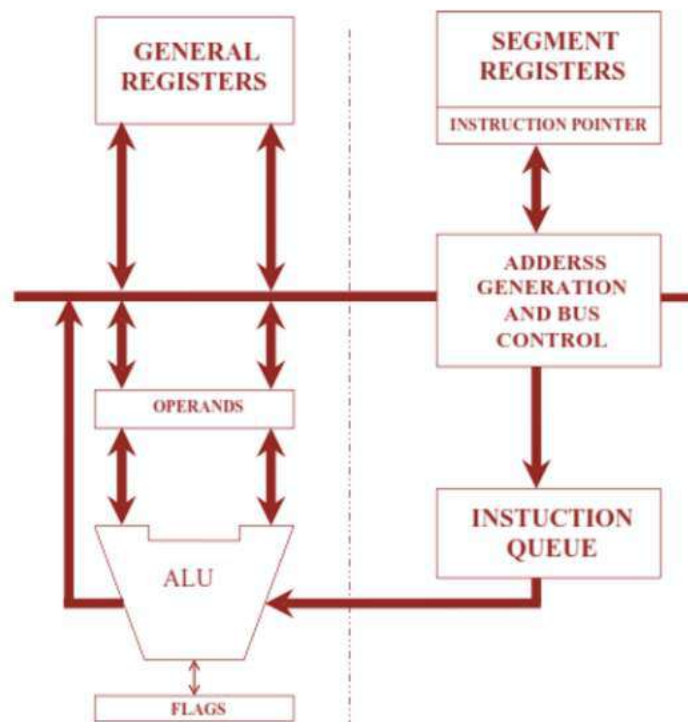
Figure7.9 Operation of 8086 Microprocessor

5.8   INTEGRATED CIRCUITS

INTRODUCTION

An integrated circuit (also called a chip) is a piece of silicon on which multiple gates have been embedded. These silicon pieces are mounted on a plastic or ceramic package with pins along the edges that can be soldered onto circuit boards or inserted into appropriate sockets. Integrated circuits (IC) are classified by number of gates contained in them. The most important integrated circuit in any computer is the Central Processing Unit, or CPU. Each CPU chip has a large number of pins through which essentially all communication in a computer system occurs.

Considerable cost savings can be made by manufacturing all of the components required for a particular circuit function on one small slice of semiconductor material (usually silicon). The resulting integrated circuit may contain as few as 10 or more than 100,000 active devices (transistors and diodes). Figure 8.1 and Figure 8.2.
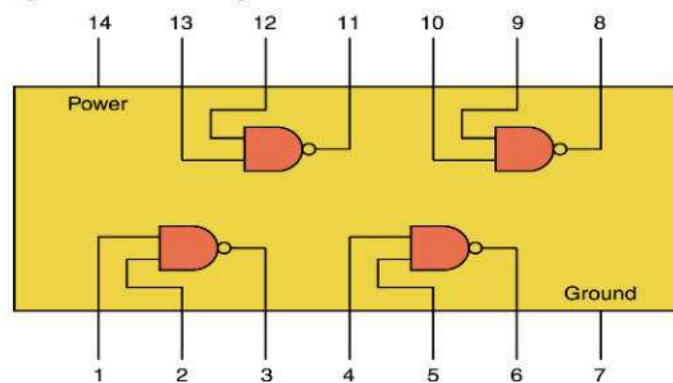
Figure 8.1 : An SSI Chip Contains Independent NAND Gates
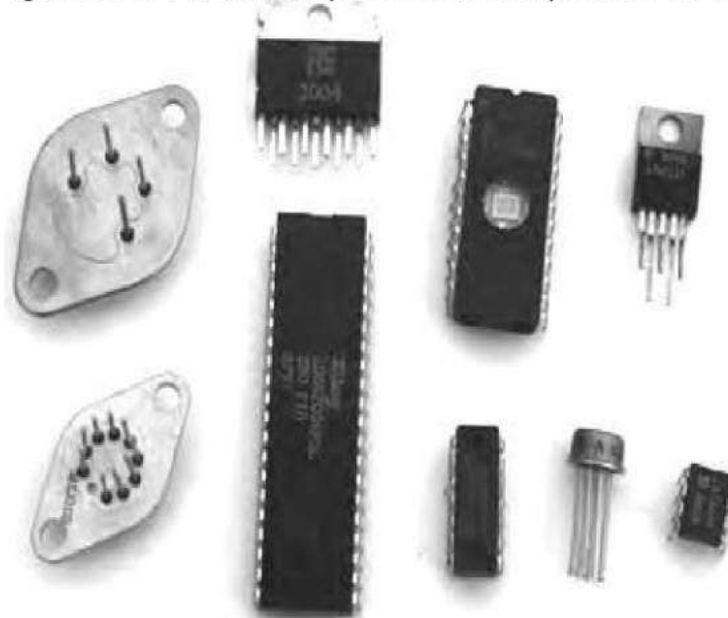
Figure 8.2: Various integrated circuits (Including Logic Gates, Operational Amplifiers and Memories)

With the exception of a few specialized applications (such as amplification at high power levels) integrated circuits have largely rendered conventional circuits (i.e. those based on discrete components such as individually packaged resistors, diodes and transistors) obsolete. Integrated circuits can be divided into two general classes, linear (analogue) and digital. Typical examples of linear integrated circuits are operational amplifiers whereas typical examples of digital integrated circuits are the logic gates and microprocessors that you met in the earlier chapters. It's worth noting that a number of integrated circuit devices bridge the gap between the analogue and digital world. Such devices include analogue to digital converters (ADC), digital to analogue converters (DAC), and timers.

Operational amplifiers are analogue integrated circuits designed for linear amplification that offer near-ideal characteristics (virtually infinite voltage gain and input resistance coupled with low output resistance and wide bandwidth). Operational amplifiers can be thought of as universal 'gain blocks' to which external components are added in order to define their function within a circuit. By adding two resistors, we can produce an amplifier having a precisely defined gain. Alternatively, with three resistors and two capacitors we can realize a low-pass filter. From this you might begin to suspect that operational amplifiers are really easy to use. The symbol for an operational amplifier is shown in Figure8.4. There are a few things to note about this.
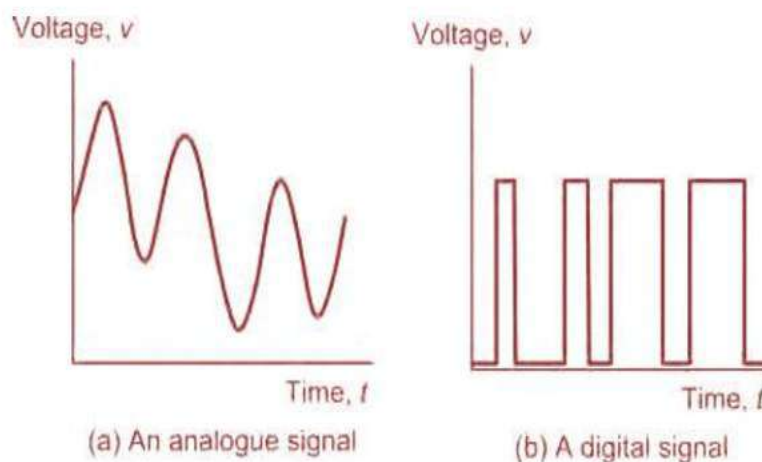
Figure 8.3: Digital and analoguesignals
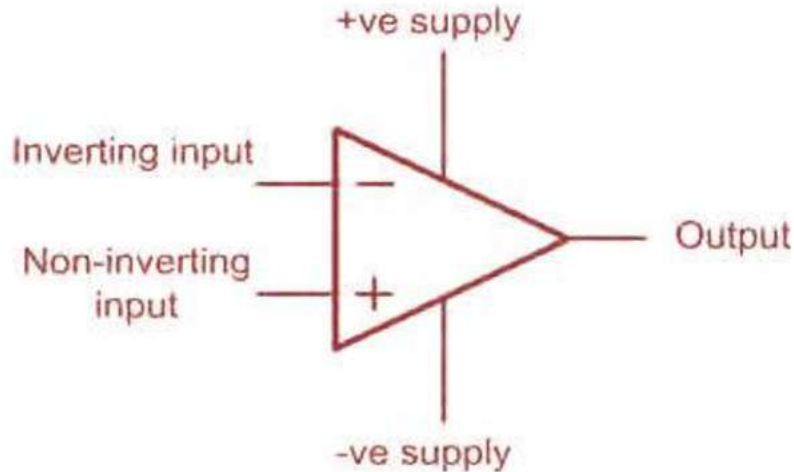
Figure 8.4 : Symbol for an operation alamplifier

The device has two inputs and one output and no common connection. Furthermore, we often don't show the supply connections – it is often clearer to leave them out of the circuit altogether. Figure 8.4, above, one of the inputs is marked '-ve' and the other is marked '+ve'. These polarity markings have nothing to do with the supply connections – they indicate the overall phase shift between each input and the output. The '+ve' sign indicates zero phase shift whilst the '-ve' sign indicates 180° phase shift. Since 180° phase shift produces an inverted (i.e., turned upside down) waveform, the '-ve' input is often referred to as the 'inverting input'. Similarly, the '+ve' input is known as the 'non-inverting' input. Most (but not all) operational amplifiers require a symmetrical power supply (of typically ± 6 V to ±15 V). This allows the output voltage to swing both positive (above 0V) and negative (below 0V). Others types of operational amplifier operate from a single supply voltage of usually between 5V and 15V.

NOTE 1 : Integrated circuits contain large numbers of individual components fabricated on a single slice of silicon. Integrated circuits are often classified as either digital (logic) or linear (analogue).

NOTE 2 : Operational amplifiers are linear integrated circuits that can be used as versatile 'gain blocks ' within a wide variety of linear circuits.

SCALE OF INTEGRATION

The relative size of a digital integrated circuit (in terms of the number of logic gates or equivalent devices that it contains) is often referred to as its scale of integration. The terminology shown in Table 8.1 is commonly used to describe the scale of these circuits.

NOTE: VLSI integrated circuits contain many thousands of components fabricated on a small piece of silicon. Each of these 'chips can replace very large numbers of conventional components. Typical examples of VLSI devices are microprocessors and memory devices.

Scale of integration	Abbreviation	Number of logic gates *	Typical examples
Small	SSI	1 to 10	Basic logic (AND, OR, NAND, NOR, etc)
Medium	MSI	10 to 100	Bus buffers and transceivers; encoders and decoders, small programmed logic arrays
Large	LSI	100 to 1,000	Large gate arrays; small memory devices
Very large	VLSI	1,000 to 10,000	Large memory devices; small microprocessors
Ultra large	ULSI	More than 100,000	Large microprocessors

Table 8.1 : Scale of Integration

5.9 MULTIPLEXING

INTRODUCTION

It is the generic term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called a Multiplexer. The multiplexer, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called "channels" one at a time to the output.

MULTIPLEXERS

MUX's, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET's or relays to switch one of the voltage or current inputs through to a single output. It is a general circuit that produces a single output signal. The output is equal to one of several input signals to the circuit. The multiplexer selects which input signal is used as an output signal based on the value represented by a few more input signals, called select signals or select control line. The control lines S0, S1, and S2 determine which of eight other input lines (D0 through D7) are routed to the output (F) .A multiplexer is a device which selects data from one of many inputs and connects this data to a common single output. A practical example is the Flight Data Recording (FDR) where the Digital Flight Data Acquisition Unit (DFDAU) receives a large number of inputs from the various aircraft parameters which have to be sampled and eventually fed on one data bus line to the FDR.

Another example is in passenger entertainment systems where the passenger can select one audio/visual channel from amongst many channels supplied to the seat. These channels (inputs) are "multiplexed" in that each input is sampled and passed in serial fashion along a data bus line. When the passenger selects the required service i.e. the film channel, then only the information on that line relevant to the film channel is selected by a 'de- multiplexer' and fed to the passenger (Figure 9.1 & 9.2)

Multiplexing can be used for both digital and analog signals, but the for each type of signal, different devices have to be used.
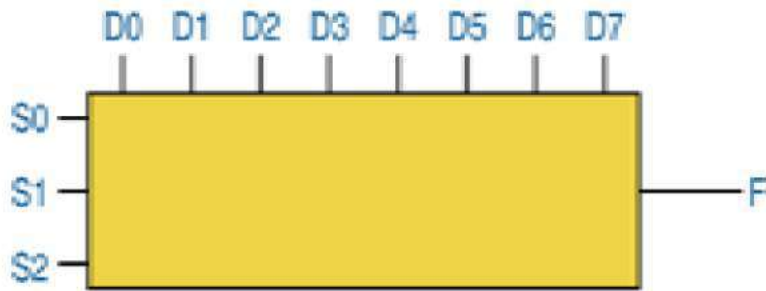
Figure 9.1: Multiplexer with Three Select Control Lines

S0	S1	S2	F
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Figure 9.2 Truth table

The difference between digital and analog multiplexing will be explained within this sub module. Figure 9.3 shows an example multiplexing as it could be used in a passenger entertainment system

The rotary switch, also called a wafer switch as each layer of the switch is known as a wafer, is a mechanical device whose input is selected by rotating a shaft. In other words, the rotary switch is a manual switch that you can use to select individual data or signal lines simply by turning its inputs "ON" or "OFF". So how can we select each data input automatically using a digital device. In digital electronics, multiplexers are also known as data selectors because they can "select" each input line, are constructed from individual Analogue Switches encased in a single IC package as opposed to the "mechanical" type selectors such as normal conventional switches and relays. They are used as one method of reducing the number of logic gates required in a circuit design or when a single data line or data bus is required to carry two or more different digital signals. For example, a single 8-channel multiplexer. Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called control lines and according to the binary condition of these control inputs, either "HIGH" or "LOW" the appropriate data input is connected directly to the output. Normally, a multiplexer has an even number of 2^n data input lines and a number of "control" inputs that correspond with the number of data inputs.

Note that multiplexers are different in operation to Encoders. Encoders are able to switch an n-bit input pattern to multiple output lines that represent the binary coded (BCD) output equivalent of the active input. Symbol for Multiplexer & Basic Multiplexing Switch (Figure 9.4 & 9.5)
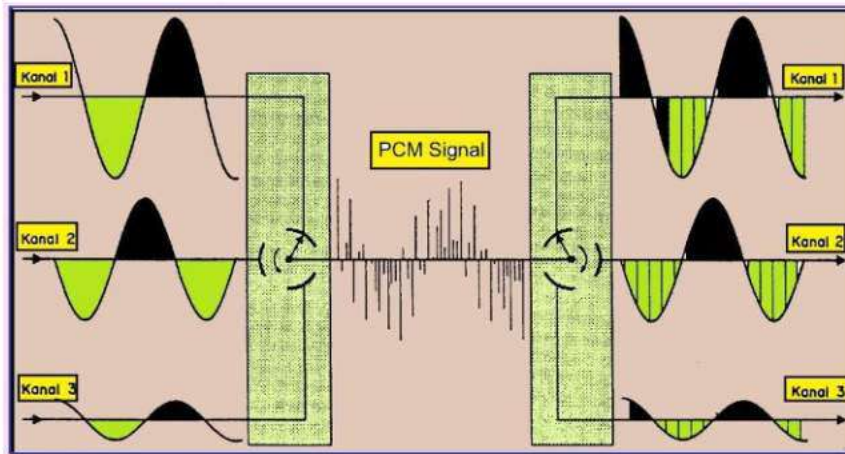
Figure9.3
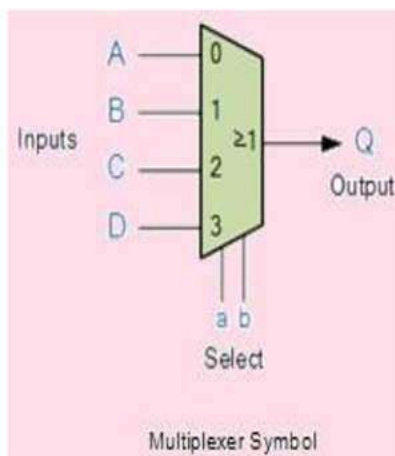
Figure9.4
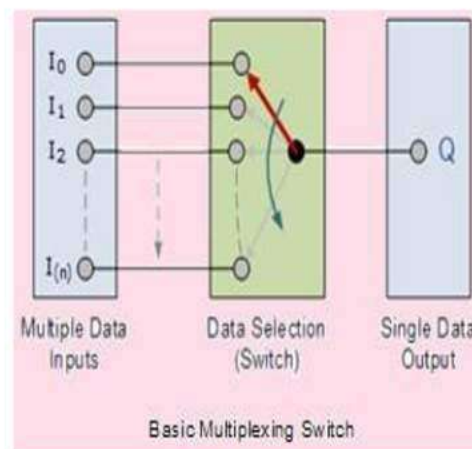
Figure9.5

Methods Of Multiplexing Operation

FREQUENCY-DIVISION MULTIPLEXING

As we have learned in the previous section, multiplexing is sending multiple signals or streams of information over a single line, at the same time in the form of a single, complex signal and then recovering the separate signals at the receiving end. Analog signals are commonly multiplexed using frequency-division multiplexing (FDM), in which the carrier bandwidth is divided into sub channels of different frequency widths, each carrying a signal at the same time in parallel. This is an older method which has been used with older telegraph systems. It is still in use in telecommunication applications e.g. directional radio systems.

WAVELENGTH DIVISION MULTIPLEXING

Dense wavelength division multiplexing (DWDM) is a technology that puts data from different sources together on an optical fiber, with each signal carried on its own separate light wavelength. Using DWDM, up to 80 (and theoretically more) separate wavelengths or channel of data can be

multiplexed into a light stream transmitted on a single optical fiber. In a system with each channel carrying 2.5 Gbps (billion bits per second), up to 200 billion bits can be delivered a second by the optical fiber. DWDM is also sometimes called wave division multiplexing (WDM). Since each channel is de-multiplexed at the end of the transmission back into the original source, different data formats being transmitted at different data rates can be transmitted together. Specifically, Internet (IP) data, Synchronous Optical Network data, and asynchronous transfer mode data can all be travelling at the same time within the optical fiber. DWDM promises to solve the "fiber exhaust" problem and is expected to be the central technology in the all-optical networks of the future.

DWDM replaces time- division multiplexing (Time-Division Multiplexing) as the most effective optical transmission method. Although TDM is the primary approach in today's networks, DWDM systems are expected to be tested and deployed in late 1998 and 1999.

TIME DIVISION MULTIPLEXING

Digital signals are commonly multiplexed using time-division multiplexing (TDM), in which the multiple signals are carried over the same in alternating time slots. As time division multiplexing is the most popular method, used also for many aircraft systems, we will study this method in detail. In TDM the data channels each occupy the same frequency band but divide the channel into time slots into which bits of signal are transmitted. The next diagram shows four data channels operating at 200bits/sec. The buffer store is a holding store until access to the data highway is signalled. The duration of each bit is 1/200s or 5ms (5 milli seconds) so an 8 bit word occupies 40ms. The common line is operated at input channel peed times the number of channels i.e., 4 x 200 = 800 bits/ sec. So each bit will have a time slot of 1.25ms. Data from the systems connected to Channels 1,2,3 and 4 are fed into a buffer store, until each store is signalled by the clock pulse to output its data onto the common line in sequence. Time Division Multiplexing is used in many aircraft systems as well as in telecommunication technologies. If many signals must be sent along a single long-distance line, careful engineering is required to ensure that the system will perform properly. An asset of TDM is its flexibility. The scheme allows for variation in the number of signals being sent along the line, and constantly adjusts the time intervals to make optimum use of the available bandwidth. The Internet is a classic example of a communications network in which the volume of traffic can change drastically from hour to hour.

MULTIPLEXER USING LOGIC GATES / DIAGRAM

We can build a simple 2-line to 1-line (2-to-1) multiplexer from basic logic NAND gates as shown in Figure 9.6.

The input A of this simple 2-1 line multiplexer circuit constructed from standard NAND gates acts to control which input (I_0 or I_1) gets passed to the output at Q. From the truth table we can see that when data select input, A is LOW (logic 0), input I_1 passes its data to the output while input I_0 is blocked. When data select A is HIGH (logic 1), input I_0 is passed to Q while input I_0 is blocked. So by the application of either a logic "0" or a logic "1" at A we can select the appropriate input with the circuit acting a bit like a single pole double throw (SPDT) switch. Then in this simple example,

the 2-input multiplexer connects one of two 1-bit sources to a common output, producing a 2-to-1-line multiplexer and we can confirm this in the following Boolean expression.

$Q = A.I_0.I_1 + A.I_0.I_1 + A.I_0.I_1 + A.I_0.I_1$

And for our 2-input multiplexer circuit above, this can be simplified too :

$Q = A.I_1 + A.I_0$

We can increase the number of data inputs to be selected further simply by following the same procedure and larger multiplexer circuits can be implemented using smaller 2-to-1 multiplexers as their basic building blocks. So for a 4-input multiplexer we would therefore require two data select lines as 4-inputs represents 2^2 data control lines give a circuit with four inputs, I_0, I_1, I_2, I_3 and two data select lines A and B as shown in Figure 9.6.e Boolean expression for this 4-to-1 Multiplexer (Figure 9.7) with inputs A to D and data select lines a, bis given as :

$Q = abA + abB + abC + abD$

In this example at any one instant in time only ONE of the four analogue switches is closed, connecting only one of the input lines A to D to the single output at Q. As to which switch is closed depends upon the addressing input code on lines "a" and "b", so for this example to select input B to the output at Q, the binary input address would need to be "a" = logic "1" and "b" = logic "0". Then we can show the selection of the data through the multiplexer as a function of the data select bits as shown in Figure 9.8.

Adding more control address lines will allow the multiplexer to control more inputs but each control line configuration will connect only ONE input to the output. Then the implementation of the Boolean expression above using individual logic gates would require the use of seven individual gates consisting of AND, OR and NOT gates as shown in Figure 9.9.

Inputs			Q
A	I_1	I_0	
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1
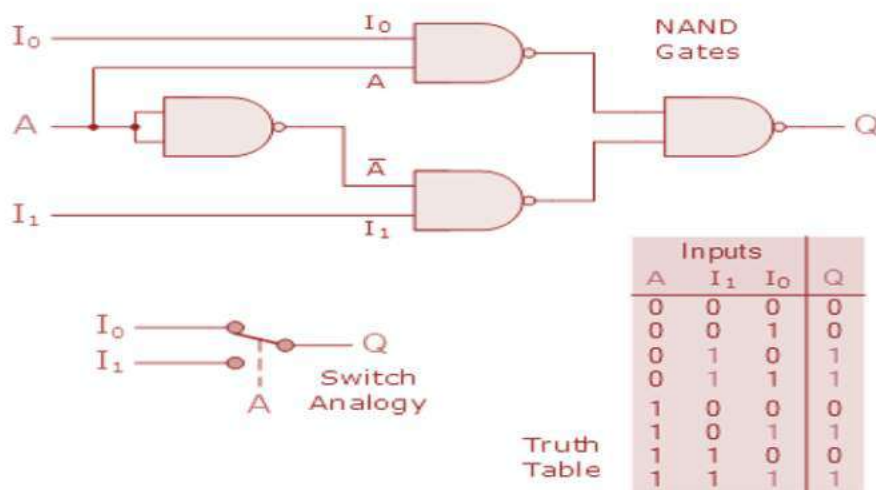
Figure 9.6: 2 Input Multiplexer Design
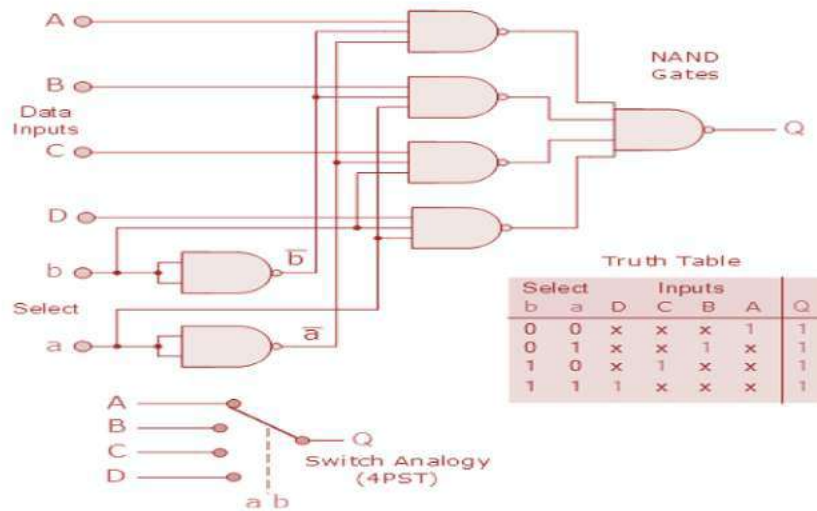
Figure 9.7: 4-to-1 Channel Multiplex

Truth Table

Select		Inputs				Q
b	a	D	C	B	A	
0	0	x	x	x	1	1
0	1	x	x	1	x	1
1	0	x	1	x	x	1
1	1	1	x	x	x	1
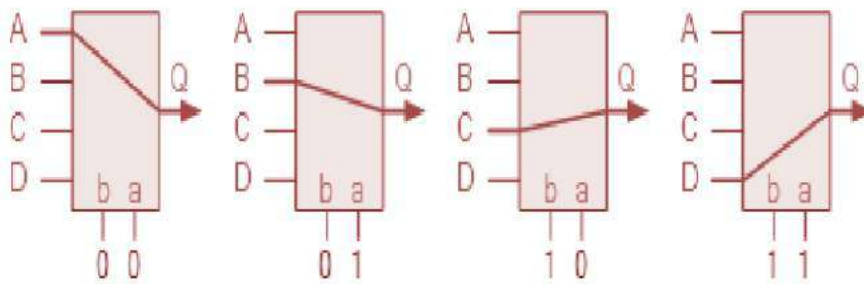
Figure 9.8: Multiplexer Input Line Selection
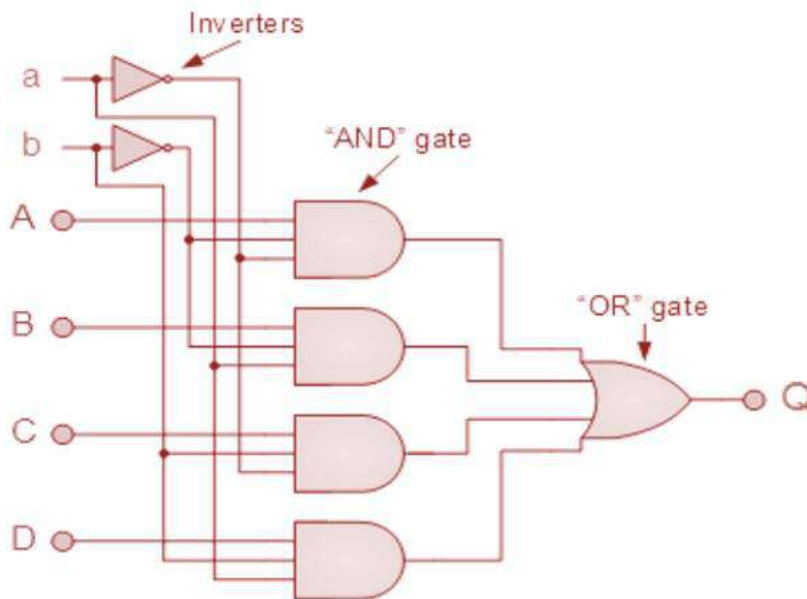
Figure 9.9 : 4 Channel Multiplexer using Logic Gate

The symbol used in logic diagrams to identify a multiplexer is as follows. Multiplexers are not limited to just switching a number of different input lines or channels to one common single output. There are also types that can switch their inputs to multiple outputs and have arrangements or 4 to 2, 8 to 3 or even 16 to 4 etc configurations and an example of a simple Dual channel 4 input multiplexer (4 to 2) is given in Figure 9.10 :

Here in this example the 4 input channels are switched to 2 individual output lines but larger arrangements are also possible. This simple 4 to 2 configuration could be used for example, to switch audio signals for stereo pre-amplifiers or mixers.
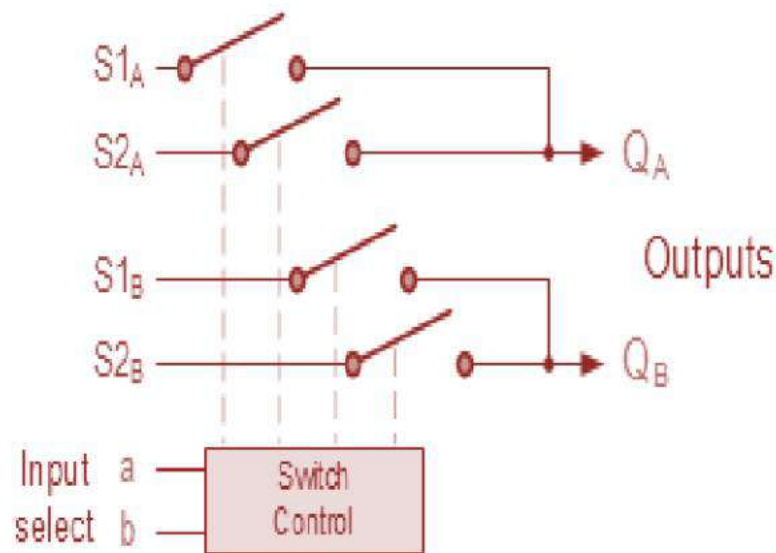
Figure 9.10: 4-to-2 Channel Multiplexer

APPLICATION OF MULTIPLEXER

• <u>ADJUSTABLE AMPLIFIER GAIN</u>

As well as sending parallel data in a serial format down a single transmission line or connection, another possible use of multi- channel multiplexers is in digital audio applications as mixers or where the gain of an analogue amplifier can be controlled digitally, for example (see in Figure 9.11).

Here, the voltage gain of the inverting operational amplifier is dependent upon the ratio between the input resistor, Rin and its feedback resistor, single 4-channel (Quad) SPST switch configured as a 4-to-1 channel multiplexer is connected in series with the resistors to select any feedback resistor to vary the value of Rf. The combination of these resistors will determine the overall gain of the amplifier, (Av). Then the gain of the amplifier can be adjusted digitally by simply selecting the appropriate resistor combination.

Like encoders, multiplexers have several inputs. However, unlike encoders, they have only one output. Multiplexers provide a means of selecting data from one of several sources. Because of this,

they are often referred to as data selectors. Switch equivalent circuits of some common types of multiplexer are shown in Fig.

9.12. The single two-way multiplexer in Fig. 9.12 (a) is equivalent to a simple SPDT (changeover) switch.

The dual two-way multiplexer shown in Fig. 9.12 (b) performs the same function but two independent circuits are controlled from the same select signal.
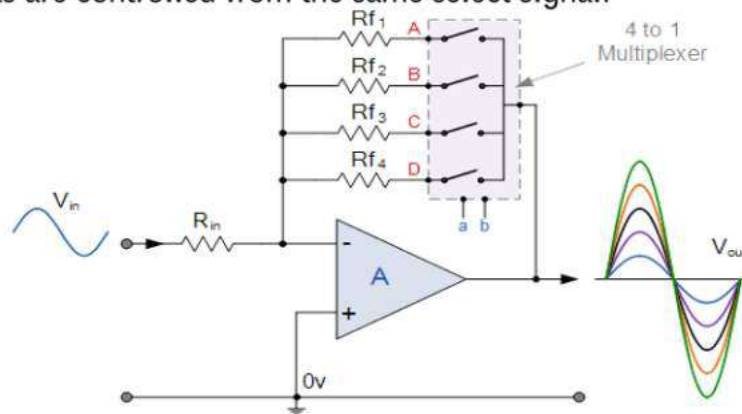
Figure 9.11: Digitally Adjustable Amplifier Gain
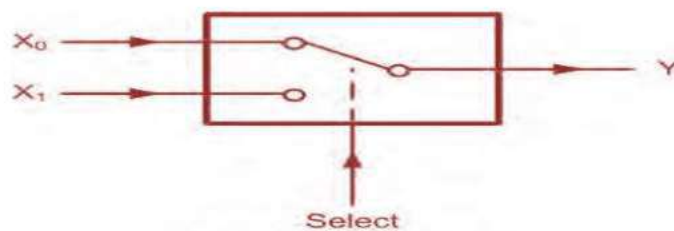
Figure 9.12 (a): Single 2 Way: Switch equivalent circuits for some common types of multiplexer or data selector
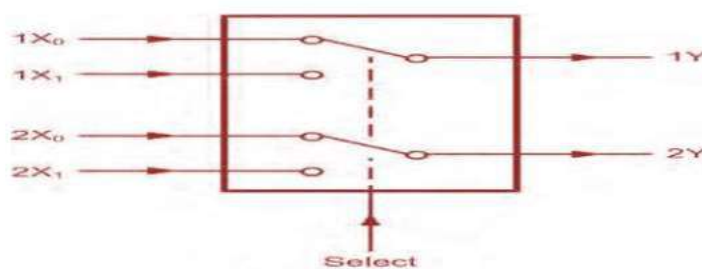
Figure 9.12 (b): Dual 2 Way : Switch equivalent circuits for some common types of multiplexer or data selector

Single four-way multiplexer is a single 4 way switch equivalent to circuits for some common types of multiplexer or data selector shown in Fig. 9.12 (c).

Note that two digital select inputs are required, A and B, in order to place the switch in its four different states. Block schematic symbols, truth tables and simplified logic circuits for two to one and four to one multiplexers are shown in Fig. 9.13 (a) to 9.13 (d).

Fig. 9.13 (c) A four to one multiplexer. The logic state of the A and B inputs determines which of the four logic inputs (X0 to X3) appears at the output.
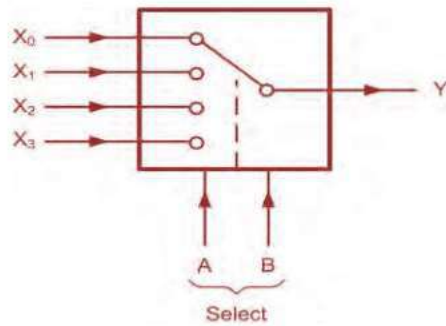
Figure 9.12 (c)
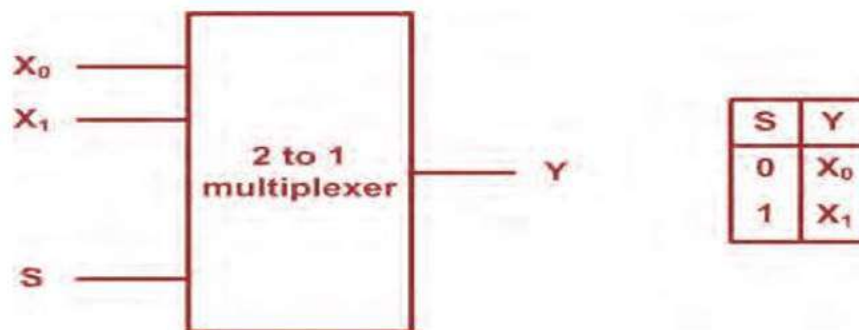
Figure 9.13 (a) : A basic two to one multiplexer arrangement with its corresponding truth
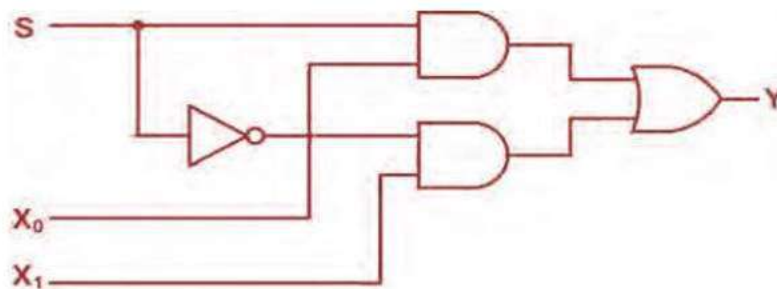
Figure 9.13 (b) : Logic circuit arrangement for the basic two to one multiplexer
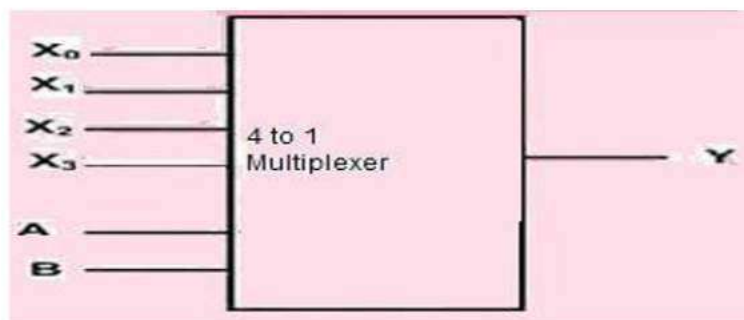
Figure 9.13(c)
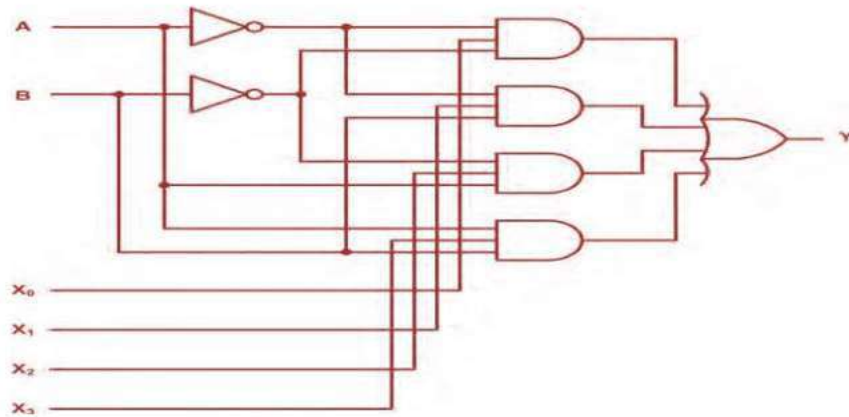
Figure 9.13(d)

NOTE

The practical realization of an eight to one and 16 to one multiplexers, the 74LS151 and 74LS150 respectively, are shown in Figures 9.14 and 9.16 respectively. These MSI devices are both implemented using low-power Schottky TTL technology and they are supplied in either plastic DIP, ceramic or SOIC packages. A typical example of the use of multiplexers and decoders is shown in the simplified block schematic of the altimeter data selector shown in Figure 9.15. This arrangement uses a dual four channel multiplexer to select corresponding clock and data streams from the four ARINC 429 bus receivers.

Pin connections for the 74LS151 eight input multiplexer (data selector)

Figure9.14

Four-channel altimeter data selector based on a dual four channel multiplexer

Figure9.15

Pin connections for the 74LS150 sixteen input multiplexer (data selector)
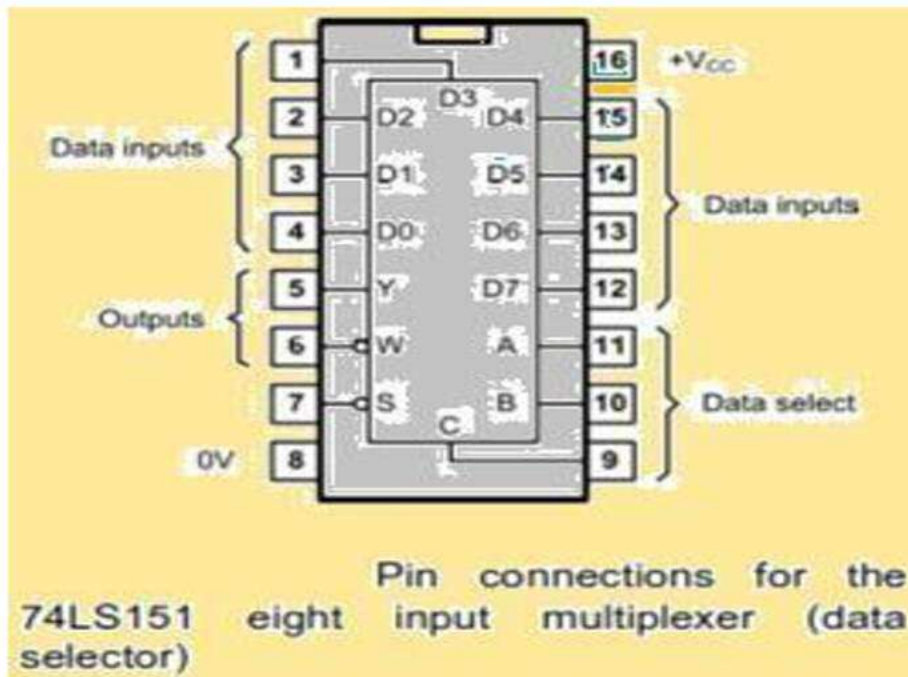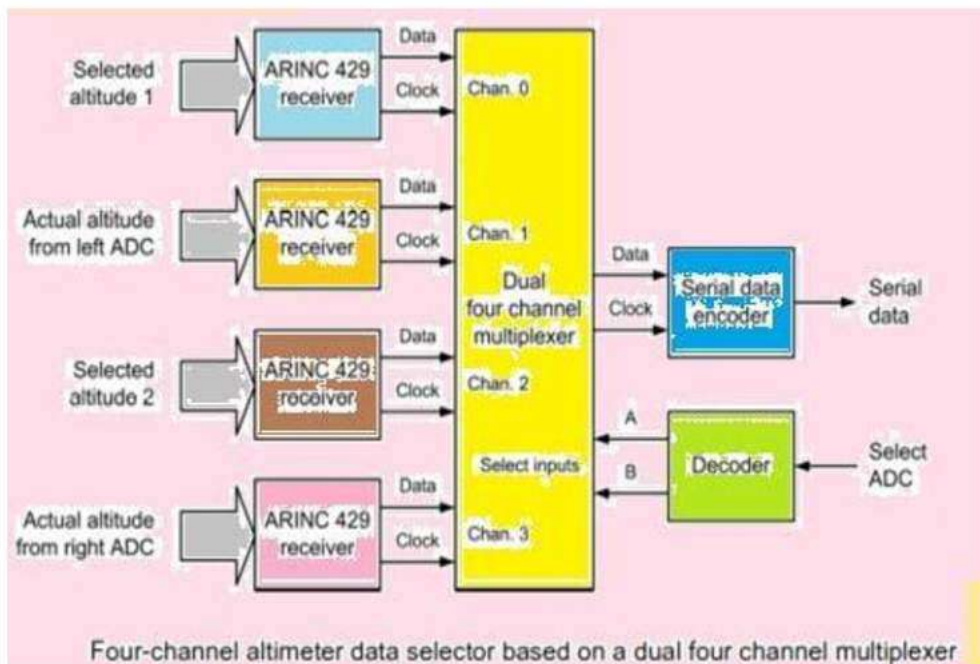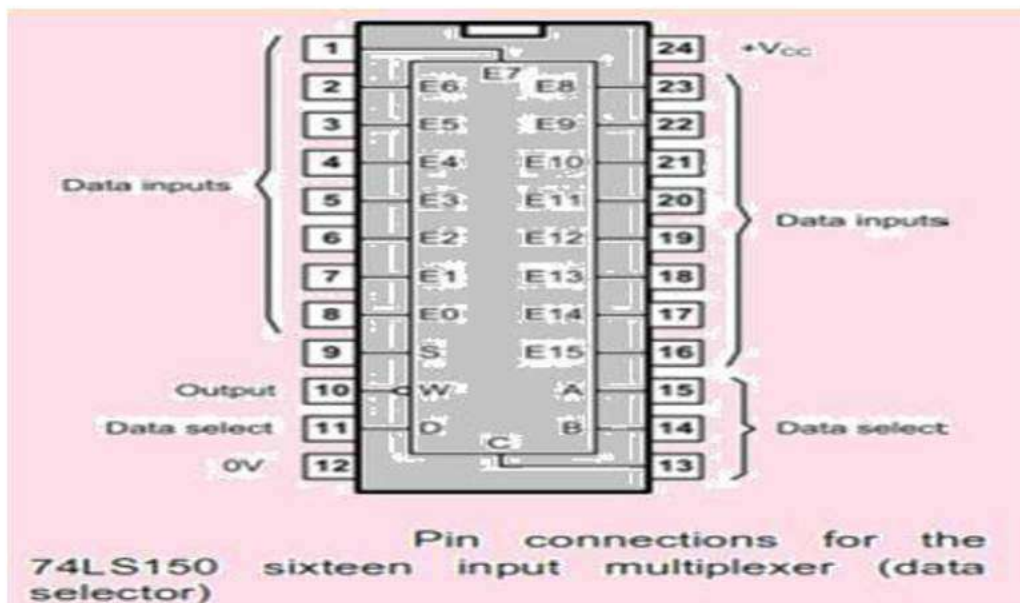
Figure9.16

DEMULTIPLEXER

A demultiplexer figure 9.17, sometimes abbreviated dmux, is a circuit that has one input and more than one output. It is used when a circuit wishes to send a signal to one of many devices. This description sounds similar to the description given for a decoder, but a decoder is used to select among many devices while a demultiplexer is used to send a signal among many devices. A demultiplexer (demux) is a decoder that only selects an output if its enable signal is asserted. A demultiplexer is used often enough that it has its own schematic symbol The truth table for a 1-to-2 demultiplexer is using our 1-to-2 decoder as part of the circuit, we can express this circuit easily as in Figure 9.18 (a & b) and 9.19. This circuit can be expanded two different ways. You can increase

the number of signals that get transmitted, or you can increase the number of inputs that get passed through.

To increase the number of inputs that get passed through just requires a larger line decoder. Increasing the number of signals that get transmitted is even easier. As an example, a device that passes one set of two signals among four signals is a "two-bit 1- to-2 de-multiplexer" as in Figure 9.20, or by expressing the circuit as in Figure 9.20 (a) and 9.20 (b) shows that it could be two one-bit 1-to-2 de-multiplexers without changing its expected behavior.
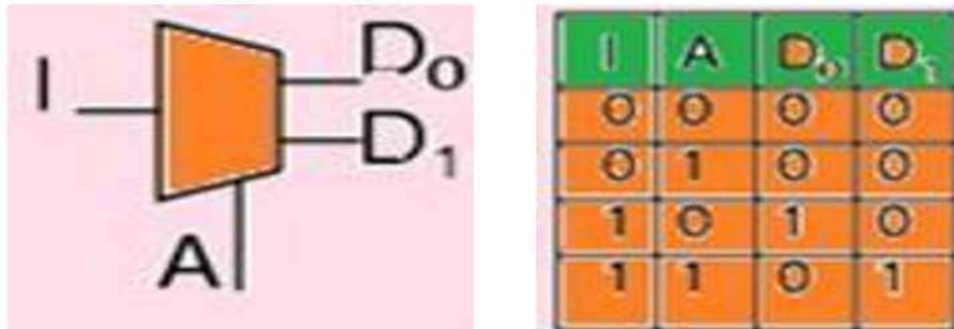
Figure 9.17 : De-multiplexer and Truth Table

5.10   FIBER OPTICS

FUNDAMENTALS OF FIBER OPTICS

The science of fiber optics deals with the transmission or guidance of light (rays or waveguide modes in the optical region of the spectrum) along transparent fibers of glass, plastic, or a similar medium. The phenomenon responsible for the fiber or light-pipe performance is the law of total internal reflection.

In Fiber optics, Fiber for this purpose is made of a very special kind of glass that is drawn into a very thin, long fiber. In some ways, this is similar to the fiberglass that is used for insulation in homes. Unlike fiberglass, however, optical fiber is made of a much different kind of glass and comes in lengths that may be many kilometers long.

Fiber Optics
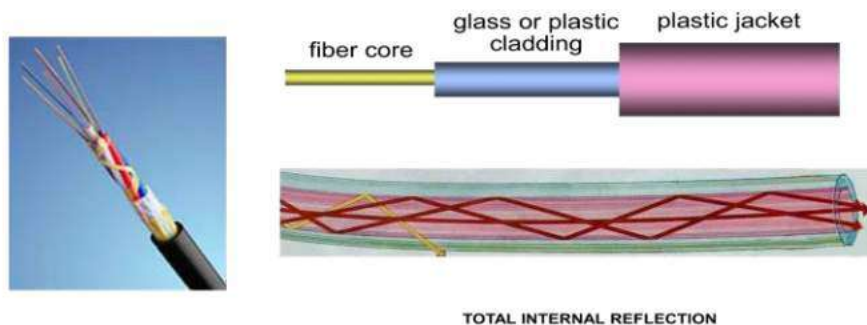
Figure 10.1

OPTICAL FIBER CONSTRUCTION

Optical fiber is composed of several elements. The construction of a fiber optic cable consists of a Two filler strands, separator tape, core, cladding, coating buffer, to prevent pulling damage during installation the Aramid strength member is added to give critical tensile (pulling) strength to the cable and outer jacket used to protects against environmental factors. The optic core is the light-carrying element at the center. It is usually made up of a combination of silica and germania. The cladding surrounding the core is made of pure silica. The cladding has a slightly lower index of refraction than the core. The lower refractive index causes the light in the core to reflect off the cladding and stay within the core.

Index of refraction is the ratio of the velocity of light in a vacuum to the velocity of light in a material. The speed of light in a vacuum is equal to 300,000,000 meters per second. The higher the index of refraction, the slower the speed of light through the material.

Index of Refraction = Light velocity (vacuum) ÷ Light velocity (material)

For example:

Air = 300,000,000 meters/second IR = 1

Glass = 200,000,000 meters/second IR = 1.5

Fiber is either single mode or multimode. Fiber sizes are expressed by using two numbers: 8/125. The first number refers to the core size in microns. The second number refers to the core size plus the cladding size combined.
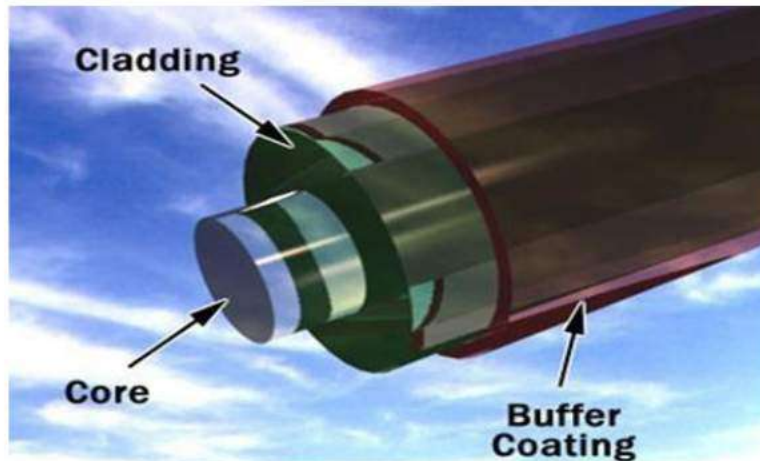
Figure 10.2

The cable has an overall diameter of about 0.2 inches and the individual optical fiber strands have a diameter of 140 μm (approx. 0.0055 inches). A protective buffer covers each fibre and

protects it during manufacture, increases mechanical strength and diameter in order to make handling and assembly easier. The buffers are coded in order to identify the fibers using colors (blue, red, green, yellow and white). The filler strands are made from polyester and are approximately 0.035 inches in diameter. A polyester separator tape covers the group of five fiber and two filler strands. This tape is manufactured from low-friction polyester and it serves to make the cable more flexible. A layer of woven Aramid (or Kevlar) yarn provides added mechanical strength and protection for the cable assembly. The outer thermoplastic jacket (usually purple in colour) is fitted to prevent moisture ingress and also to provide insulation.
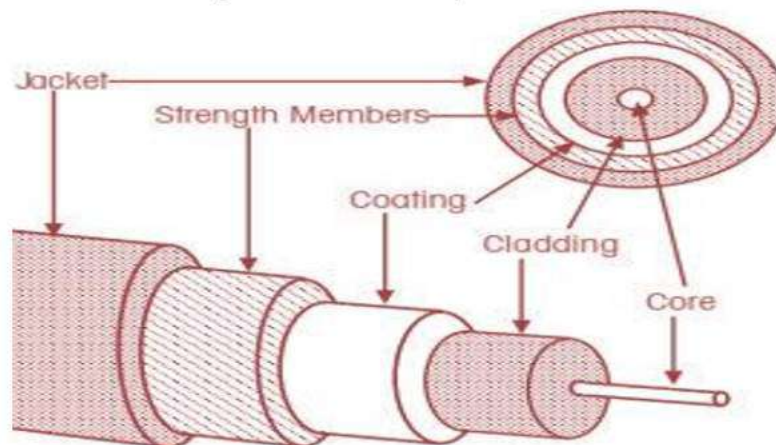
Figure 10.3
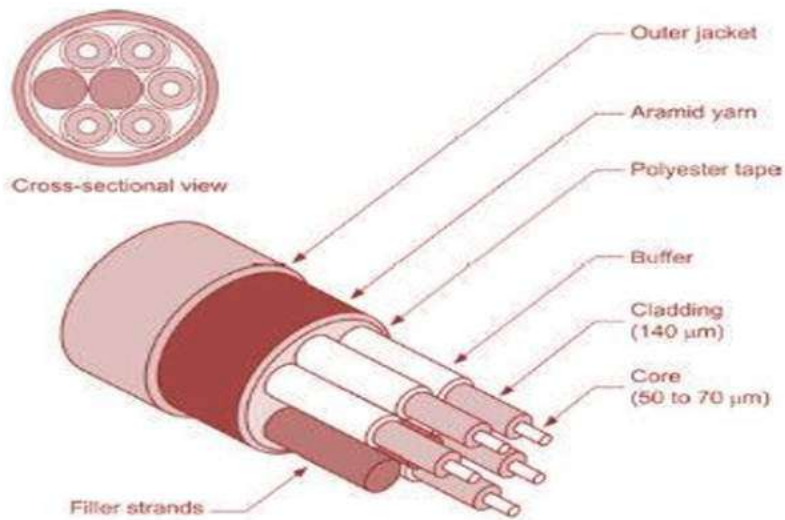
Figure 10.4

TOTAL INTERNAL REFLECTION

A ray of light, incident upon the interface between two transparent optical materials having different indices of refraction, will be totally internally reflected (rather than refracted) if

1. The ray is incident upon the interface from the direction of the more dense material and
2. The angle made by the ray with the normal to the interface is greater than some critical angle,

The latter being dependent only on the indices of refraction of the media (See Figure 10.5).
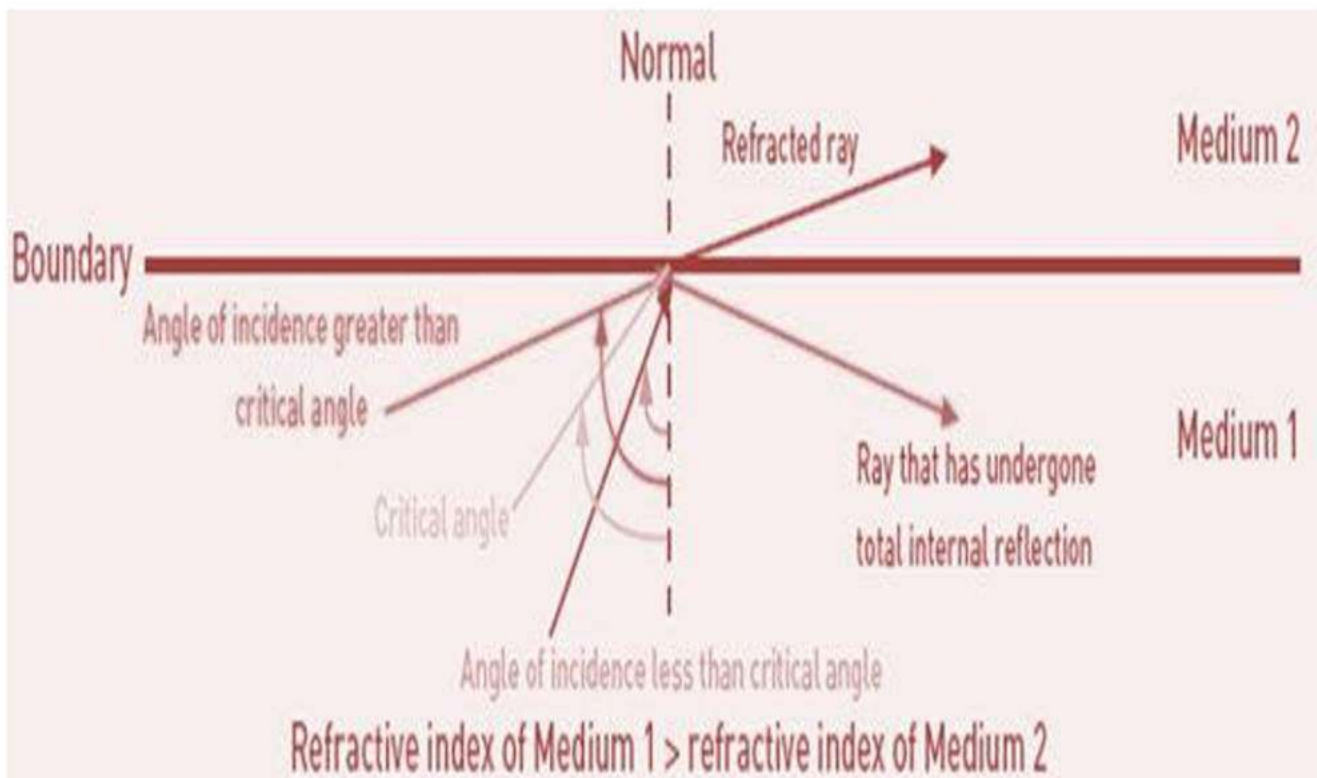
Figure 10.5
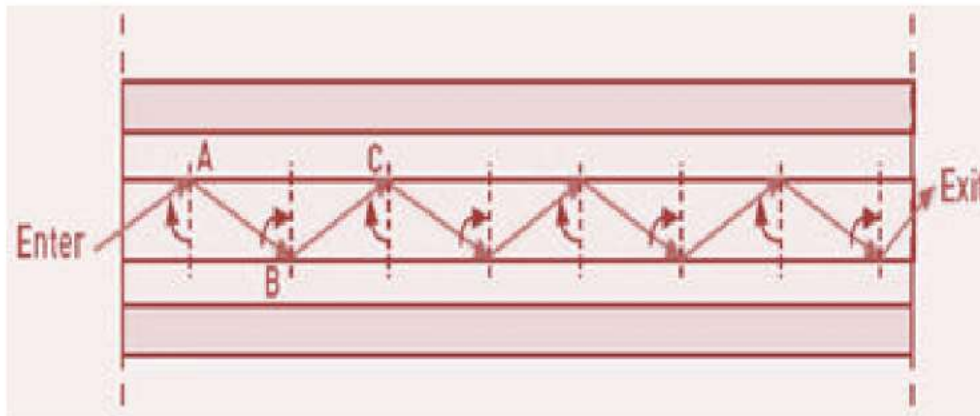
Figure 10.6
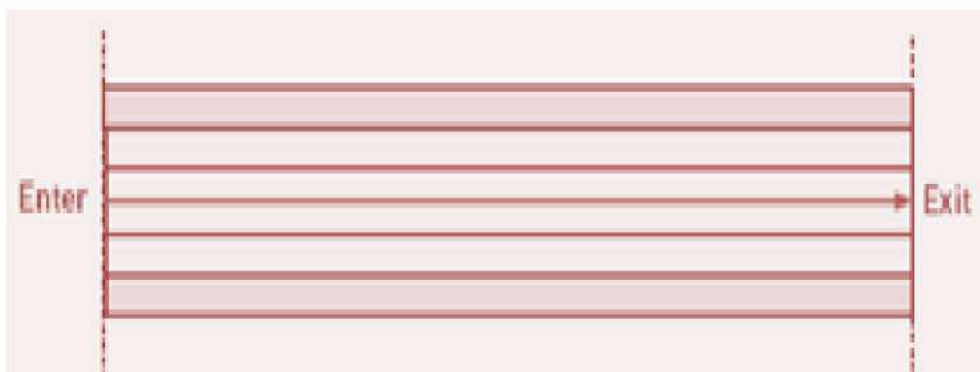
Figure 10.7
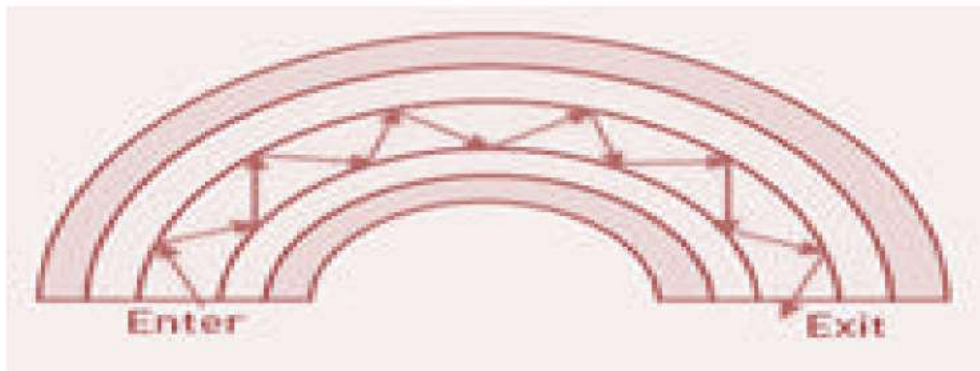
Figure 10.8

As indicated in Figure 10.1, the angle of reflection is equal to the angle of incidence. (By definition, the angle is that measured between the ray and the normal to the interface at the point of reflection.) An off-axis ray of light traversing a fiber 50 microns in diameter may be reflected 3000 times per foot of fiber length. This number increases in direct proportion to diameter decrease. Total internal reflection between two transparent optical media results in a loss of less than 0.001 percent per reflection; thus a useful quantity of illumination can be transported. An aluminum mirror cladding on a glass fiber core would sustain a loss of Approximately 10 percent per reflection, a level that could not be tolerated in practical fiber optics.

Light is transmitted down the length of a fiber at a constant angle with the fiber axis. Scattering from the true geometric path can occur, however, as a result of true geometric path can occur, however, as a result of

1. Imperfections in the bulk of the fiber;
2. Irregularities in the core/clad interface of the fiber; and
3. Surface scattering upon entry.

In the first two instances, light will be scattered in proportion to fiber length, depending upon the angle of incidence. To be functional, therefore, long fibers must have an optical quality superior to that of short fibers. surface scattering occurs readily if optical polishing has not produced a surface that is perpendicular to the axis of the fiber; pits, scratches, and scuffs diffuse light very rapidly. The speed of light in matter is less than the speed of light in air, and the change in velocity that occurs when light passes from one medium to another results in refraction.

It should be noted that a portion of the light incident on a boundary surface is not transmitted but is instead reflected back into the air. That portion that is transmitted is totally reflected from the sides, assuming that the angle is less than the critical angle (See Figure 10.1). The relationship between the angle of incidence 'i' and the angle of refraction 'r' is expressed by Snell's law as

$$N1 \times Sin\ (i) = N2 \times Sin\ (r)$$

Where, N1 is the index of refraction of air and N2 the index of refraction of the core. Since N1=1 for all practical purposes, the refractive index of the core becomes

$$N2 = Sin\ (i)\ /\ Sin\ (r)$$

TERMS AND WORDS USED IN FIBRE OPTICS

Cladding	A sheathing or covering, usually of glass, fused to the core or higher-index material.
Collimated Light	Rays of light traveling as a parallel beam.
Cross Talk	The observable leakage of light from one fiber to another. The expression is sometimes understood to include light transferred by scattering defects but usually refers only to simple electromagnetic tunneling; it is not normally construed to include neither light outside the numerical aperture nor light in the webbing, both of which migrate. Cross talk can be eliminated or decreased by increasing cladding thickness, which also increases packing-fraction transmission loss.
De collimated	Light
Light	Boundary defects.
Depth of Focus	The perpendicular distance from a surface at which an image can be resolved.
Dispersion	A measure of the change in refractive index with wavelength for a given material. In lens optics, dispersion leads to chromatic aberrations; in fiber optics, it affects only numerical aperture and field angle.

Edge Response	A measure of the image resolution and contrast properties of a fiber optics system.
Electron Amplification	The multiplication of electrons from a secondary- emission material, caused by a primary electron striking a surface with enough force to dislodge additional electrons.
Extramural Absorption Cladding	— A second cladding of opaque material commonly applied around each fiber in an optical mosaic to absorb light outside the acceptance angle.
Meridional Ray	A ray that passes through the axis of a fiber while being internally reflected (in contrast with a skew ray).
Modulation Transfer Function	A mathematical expression that reflects the ability of a system to transport information bits the sizes of which are usually expressed in line pairs per millimeter.
Multi fiber	A coherent bundle of fused single fibers that behaves mechanically like a single glass fiber.
Single Fiber	A filament of optical material, glass or plastic, usually drawn with a lower-index cladding.
Skew Ray	A ray that never intersects the axis of a fiber while being internally reflected (in contrast with a meridional ray).
Striae	Spatial variations in the index of refraction in non homogeneous glass.
Fiber Optics	The technique of conveying light through optical fibers.
Optical Fibers	(Or optical waveguides, or light pipes) thin glass or plastic flexible rods through which light can propagate. These consist of an inner core and an outer cladding, and are found inside fiber-optic cables.
Data Link	A communication link that allows the transfer of digital data.
Handshaking	A method of data-flow control between two stations during the exchange of information.
Manchester	A method of bi phase line coding where data bits are combined with the bit clock through an exclusive-OR bit time.
FPGA	A high-density integrated-circuit (IC) that can be user-configured to create a custom IC with user- defined logic functions.
Infrared	A form of radiant energy with wavelengths between 770 nm and 1 mm, which is just below the visible light region of the electromagnetic spectrum; a type of invisible light.
IRED	An LED type of output transducer that emits infrared light instead of visible light when forward biased.

Multimode Fibers	Types of optical fibers that provide many propagation paths for light. They are used with an LED light source
Simplex Cables	A type of fiber-optic cable that contains only one optical fiber.
Phototransisto r	A light-sensitive transistor whose collector current is directly related to light intensity.
Photodiode	Alight-sensitive diode whose conduction is directly related to Light intensity.

ADVANTAGES

1	Extremely High Bandwidth	No other cable-based data transmission medium offers the bandwidth that fiber does.
2	Easy to Accommodat e Increasing Bandwidth	Using many of the recent generations of fiber optic cabling, new equipment can be added to the inert fiber cable that can provide vastly expanded capacity over the originally laid fiber. DWDM, or Dense Wavelength Division Multiplexing, lends fiber optic cabling the ability to turn various wavelengths of light traveling down the fiber on and off at will. These two characteristics of fiber cable enable dynamic network bandwidth provisioning to provide for data traffic spikes and lulls.
3	Resistance to Electromagneti c Interference	Fiber has a very low rate of bit error (10EXP-13), As a result of fiber being so resistant to electromagnetic interference. Fiber-optic transmission Is virtually noise free.
4	Early Detection of Cable Damage and Secure Transmissions	Fiber provides an extremely secure transmission medium, as there is no way to detect the data being transmitted by "listening in" to the electromagnetic energy "leaking" through the cable, as is possible with optical network and by carefully measuring the time it takes light to reflect down the
		Fiber, splices in the cable can be easily detected. When high freq signal are propagated through convention coaxial cable ,it loss half of its power only after a few hundred meters where as the optical fiber loss the sauce amount of power in 15km or more. Thus repeater will be required at very long distance.
5	T/N Rate	T/N is possible on optical fiber 10GB/sec while in coaxial cable is 1GB/sec.

6	Flexibility	Because of very small size and light in weight and large Flexibility, it produces a number of advantages over copper wires at the installation time.
7	Grounding Protection	As the fiber optic has no electrical conductivity, therefore Grounding and protection are not necessary.
8	Insensitivity to EMI	Do not sense Interference such as when a one wire induces some of its signal to another.
9	Lose of Light	Fiber do not lose any light, therefore the transmission is also secure and cannot be disturbed.
10	Lack of Electrical Signals	In the fiber there is a lack of electrical signal, so it cannot shock or other hazards. This makes fibers suitable for work in explosive atmospheres.
11	Installation	Easy to install and Compatibility with digital technology.
12	Light and Small	Lightness and small size of the cable, capable of carrying a large number of signals.

DISADVANTAGES

1. INSTALLATION COSTS, WHILE DROPPING, ARE STILL HIGH

Despite the fact that fiber installation costs are dropping by as much as 60% a year, installing fiber optic cabling is still relatively costly. As installation costs decrease, fiberis expanding beyond its original real and major application in the carrier backbone and is moving into the local loop, and through technologies such as FTTx (Fiber to the Home, Premises, etc,) and PONs (Passive Optical networks), enabling subscriber and end user broadband access.

2. SPECIAL TEST EQUIPMENT IS OFTEN REQUIRED

The test equipment typically and traditionally used for conventional electron-based networking is of no use in a fiber optic network. Equipment such as an OTDR (Optical Time Domain Reflect meter) is required, and expensive, specialized optical test equipment such as optical probes are needed at most fiber endpoints and connection nexuses in order to properly provide testing of optical fiber.

3. SUSCEPTIBILITY TO PHYSICAL DAMAGE

Fiber is a small and compact cable, and it is highly susceptible to becoming cut or damaged during installation or construction activities. Because of this, when fiber optic cabling is chosen as the transmission medium, it is necessary to address restoration, backup and survivability.

4. PRICE

Even though the raw material for making optical fibers, sand, is abundant and cheap, optical fibers are still more expensive per meter than copper. Although, one fiber can carry many more signals than a single copper cable and the large transmission distances mean that fewer expensive repeaters are required.

5. FRAGILITY

Optical fibers are more fragile than electrical wires.

6. AFFECTED BY CHEMICALS

The glass can be affected by various chemicals including hydrogen gas (a problem in underwater cables).

7. OPAQUENESS

Despite extensive military use it is known that most fiber become opaque when exposed to radiation.

8. REQUIRES SPECIAL SKILLS

Optical fiber cannot be joined together as a easily as copper cable and requires additional traning of personnel and expensive precision splicing and measurement equipment.

9. The joining of fiber optic cables need greater care because if the Joining is not correct; a lot of attenuation will produce in high Wave length.

10. As the fiber optics have no electrical conductivity, therefore additional Copper cable is not used with optical fiber to provide power supply to the repeaters.

11. The installation cost is very high as compare to the other types of T/N lines.

PROPAGATION IN OPTICAL FIBRES

Essentially, an optical fiber consists of a cylindrical silica glass core surrounded by further glass cladding. The fiber acts as a channel (or waveguide) along which an electromagnetic wave can pass with very little loss. Fiber optics is governed by the fundamental laws of reflection and refraction. For example, when a light wave passes from a medium of higher refractive index to one of lower refractive index, the wave is bent towards the normal, as shown in Figure 9 (a). Conversely, when travelling from a medium of lower refractive index to one of higher refractive index, the wave will be bent away from the normal, as shown in Figure 9 (b).

(a) Refraction towards the normal ($n_2 > n_1$)

(b) Refraction away from the normal ($n_2 < n_1$)
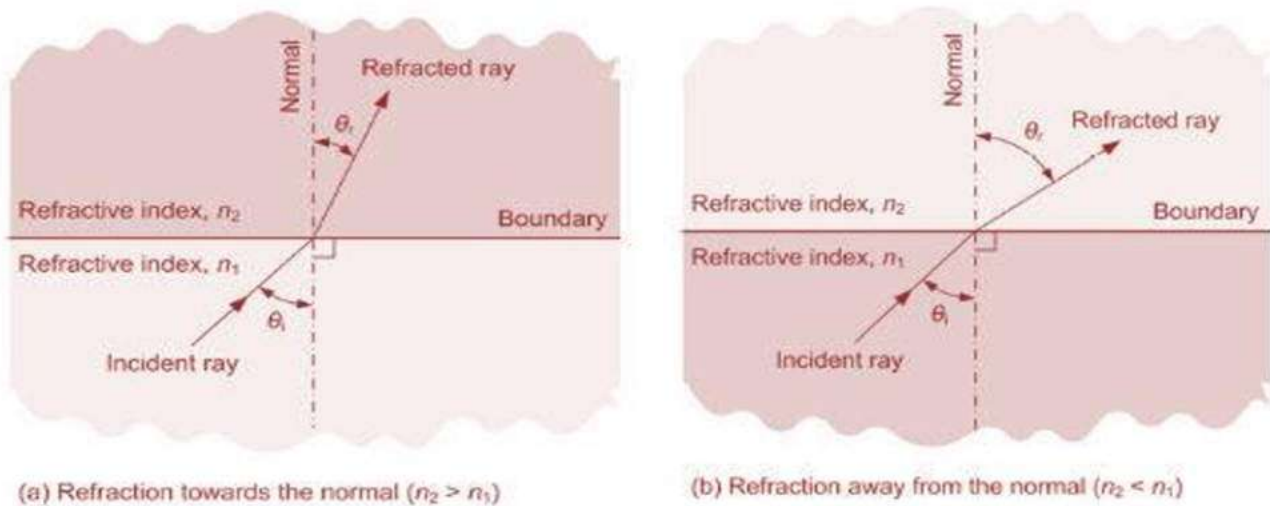
Figure 10.9: Refraction of a beam of light at a boundary

In latter case, some of the incident light will be reflected at the boundary of the two media and, as the angle of incidence is increased, the angle of refraction will also be increased until, at a critical value, the light wave will be totally reflected (i.e. the refracted ray will no longer exist, as shown in

(a) Angle of incidence less than the critical angle ($\theta < \theta_c$)

(c) Angle of incidence greater than the critical angle ($\theta > \theta_c$)

(b) Angle of incidence equal to the critical angle ($\theta = \theta_c$)

(d) Multiple rays travelling by means of total internal reflection
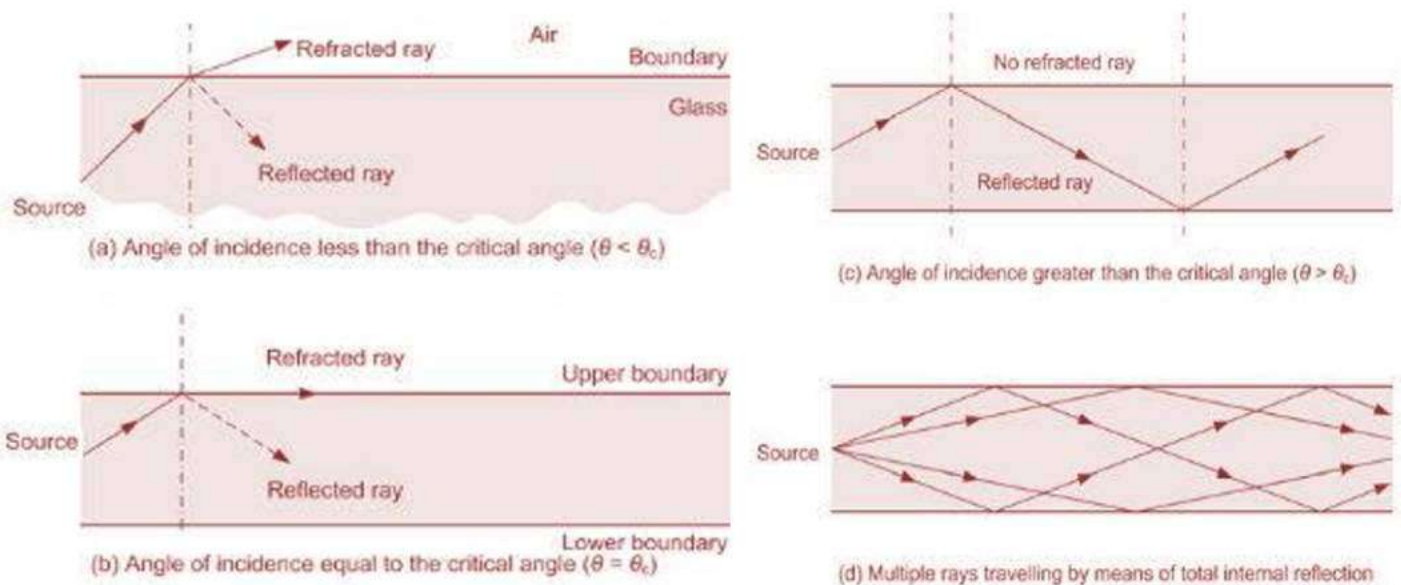
Figure 10.10: Refraction and reflection at different angles of incidence

The angle of incidence at which this occurs is known as the critical angle, θ_c. The value of θ_c depends upon the absolute refractive indices of the media and is given by:

Where n_1 and n_2 are the refractive indices of the more dense and less dense media respectively Optical fibers are manufactured by drawing silica glass from the molten state and they are thus of cylindrical construction. The more dense medium (the core) is surrounded by the less dense medium (the cladding). Provided that the angle of incidence of the input wave is larger than the critical angle, the light wave will propagate inside the core by means of a series of total internal reflections. Any other light waves that are incident on the upper boundary at an angle θ_c greater than θ will also

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propagate along the inner medium. Conversely, any light wave that is incident upon the upper boundary with θ less than θ_c will pass into the outer medium and there be lost by scattering and / or absorption.

CONE OF ACCEPTANCE

The cone of acceptance (Fig. 10.11) is the complete set of angles which will be subject to total internal reflection. Rays entering from the edges will take a longer path through the fibre but will travel faster because of the lower refractive index of the outer layer. The numerical aperture determines the and width of the fibre and is given by:

Numerical Aperture, $A = \sin \theta_a$
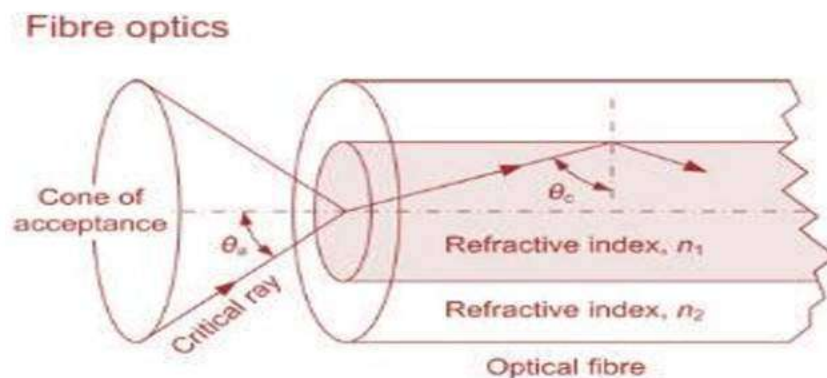
Figure 10.11: Cone of Acceptance

Clearly, when a number of light waves enter the system with differing angles of incidence, a number of waves (or modes) are able to propagate. This multimode propagation is relatively simple to achieve but has the attendant disadvantage that, since the light waves will take different times to pass through the fibre, the variation of transit time will result in dispersion which imposes an obvious restriction on the maximum bit rate that the system will support. There are two methods for reducing multimode propagation. One uses a fibre of graded refractive index whilst the other uses a special single mode (or monomode) fibre. The inner core of this type of fibre is reduced in diameter so that it has the same order magnitude as the wavelength of the incident wave. This ensures that only one mode will successfully propagate.

LOSSES OR ATTENUATION

There are number of causes for the loss in fibre optics including
- Absorption losses due to impurities in the Fiber material, absorption, scattering in the core (due to non-homogeneity of the refractive index), scattering at the core/ cladding boundary.
- Material or Rayleigh scattering losses due to microscopic irregularities in the Fiber.
- Chromatic or wavelength dispersion because of the use of a non-monochromatic source.
- Radiation losses caused by bends and kinks in the Fiber.

- Pulse spreading or modal dispersion due to rays taking different paths down the Fiber (ms/km).
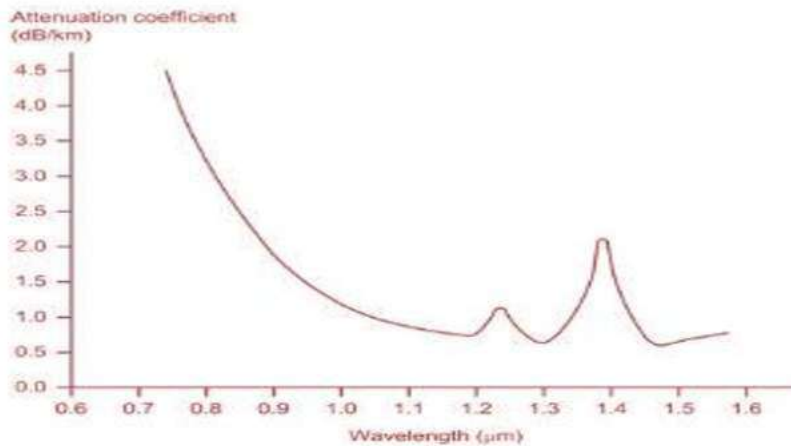
Figure 10.12: Attenuation

In general, the attenuation of a good quality fiber can be expected to be less than 2 dB per km at a wavelength of 1.3 μm (infra-red). Hence a 50 m length of fiber can be expected to exhibit a loss of around 0.1 dB. Whereas the attenuation coefficient of an optical fiber is largely dependent upon the quality and consistency of the glass used for the core and cladding, the attenuation of all optical fibers varies widely with wavelength. The typical attenuation/wavelength characteristic for an mono mode fiber is shown in Figure 10.12.

It should be noted that the sharp peak at about 1.39 μm arises from excess absorption within the mono mode fiber. Mono mode fibers are now a common feature of ground-based high speed data communication systems and manufacturing techniques have been developed that ensure consistent and reliable products with low attenuation and wide operational bandwidths. However, since mono mode fibers are significantly smaller in diameter than their multimode predecessors (Fig. 10.13 a & b), a consistent and reliable means of cutting, surface preparation, alignment and Inter connection is essential, and for this reason slower multimode fibers are still prevalent in current aircraft designs.

(a) Multimode fibre

Figure 10.13 (a)

(b) Monomode fibre
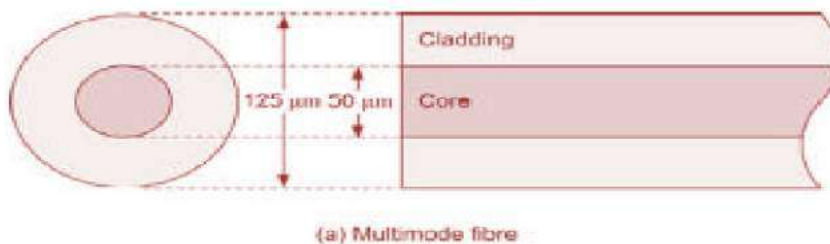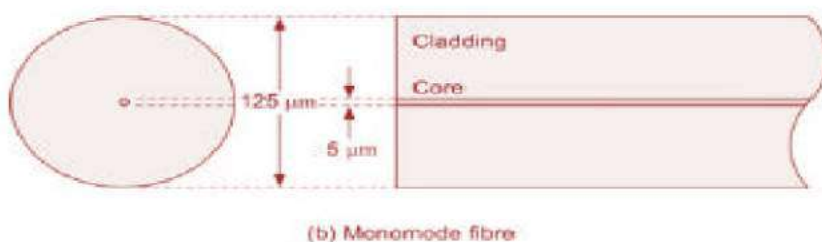
Figure 10.13 (b)

DISPERSION

A simple one-way (simplex) fiber optic data link is shown in Figure 10.14. The optical transmitter consists of an infra-red light emitting diode (LED) or low-power semiconductor laser diode coupled directly to the optical fiber.
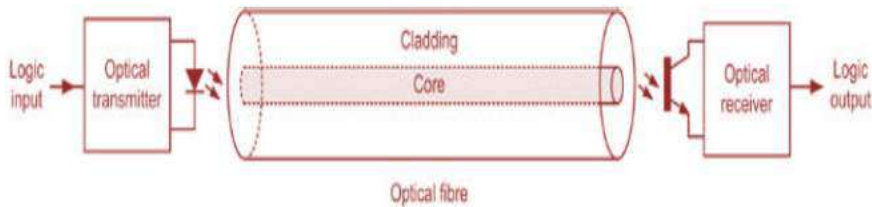
Figure 10.14: A Simple One-Way Fiber Optic Data Link
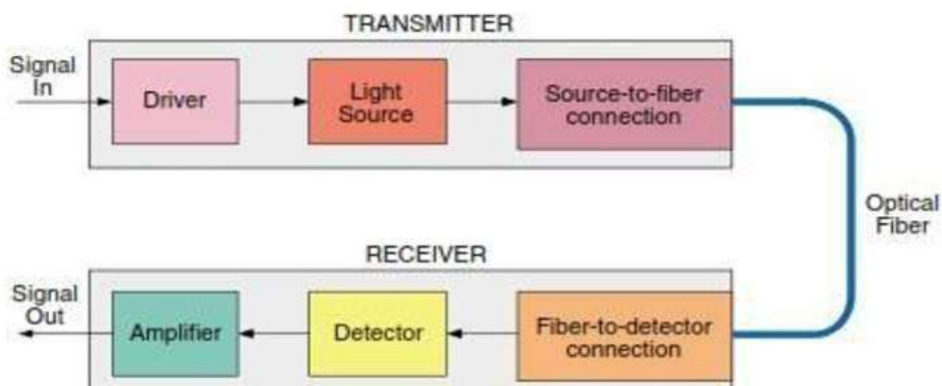
Figure 10.15

The diode is supplied with pulses of current from a bus interface. These pulses of current produce equivalent pulses of light that travel along the fibre until they reach the optical receiver unit. The optical receiver unit consists of a photodiode or phototransistor that passes a relatively large current when illuminated and negligible current when not. The pulses of current at the transmitting end are thus replicated at the receiving end. The maximum data rate (and consequently the bandwidth) of the optical data link depends on the ability of the system shown in Figure 14 to faithfully reproduce a train of narrow digital pulses. Unfortunately, in a multimode fibre different modes travel at different velocities, as shown earlier. This phenomenon is known as dispersion and it has the effect of stretching the output pulse, as shown in Figure 10.16.
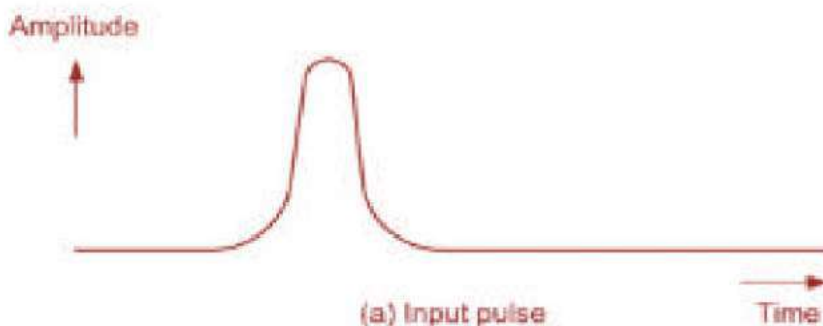
Figure 10.16

BANDWIDTH

When digital data is supplied to the optical transmitter, the stretching of pulses imposes an upper limit on the rate at which the pulses can be transmitted. In other words, the data rate is determined by the amount of dispersion simply because a longer bit interval means fewer bits can be transmitted in the same unit of time.

(a) Fibre output with no dispersion

Figure 10.17 (a)

(b) Fibre output with dispersion
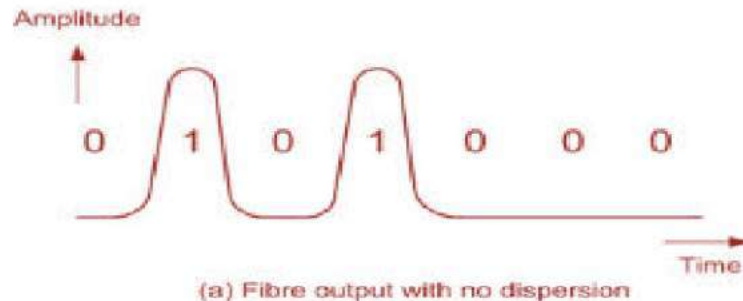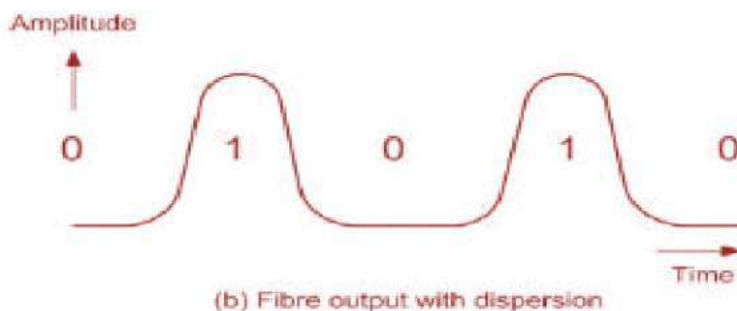
Figure 10.17: Effect of dispersion on the width of pulses received from an optical fibre

Figure 10.17 (b)

FIBRE OPTIC CONNECTORS

To be useful, a connector has to have certain properties such as
- A connector has to allow as much light to get through as possible.
- A connector has to be rugged.
- A connector should allow the same amount of light through each time it is disconnected and reconnected.
- A connector should be easy and simple to install.
- Precise   and   repeatable   (even after   numerous   mating operations)
- Suitable for installation without specialist tooling
- Low loss
- Low cost.

Whilst the loss exhibited by a connector may be quoted in absolute terms, it is often specified in terms of an equivalent length of optical fiber. If, for example, six connectors are used on a cable run and each connector has a loss of 0.5 dB the total connector loss will be 3 dB. This is equivalent to

several kilometers of low-loss fiber. A typical fiber optic cable connector arrangement is shown in Figure 10.18. This comprises Alignment keys and grooves, Guide pins and cavities, Colored alignment bands, three start threads, each connector has alignment keys on the plug and matching alignment grooves on the receptacle.
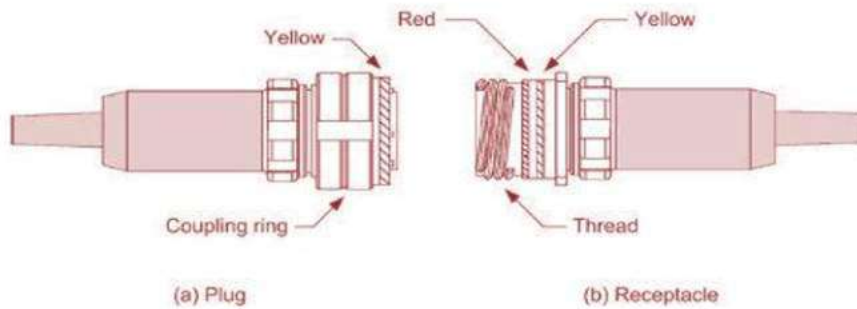
Figure 10.18
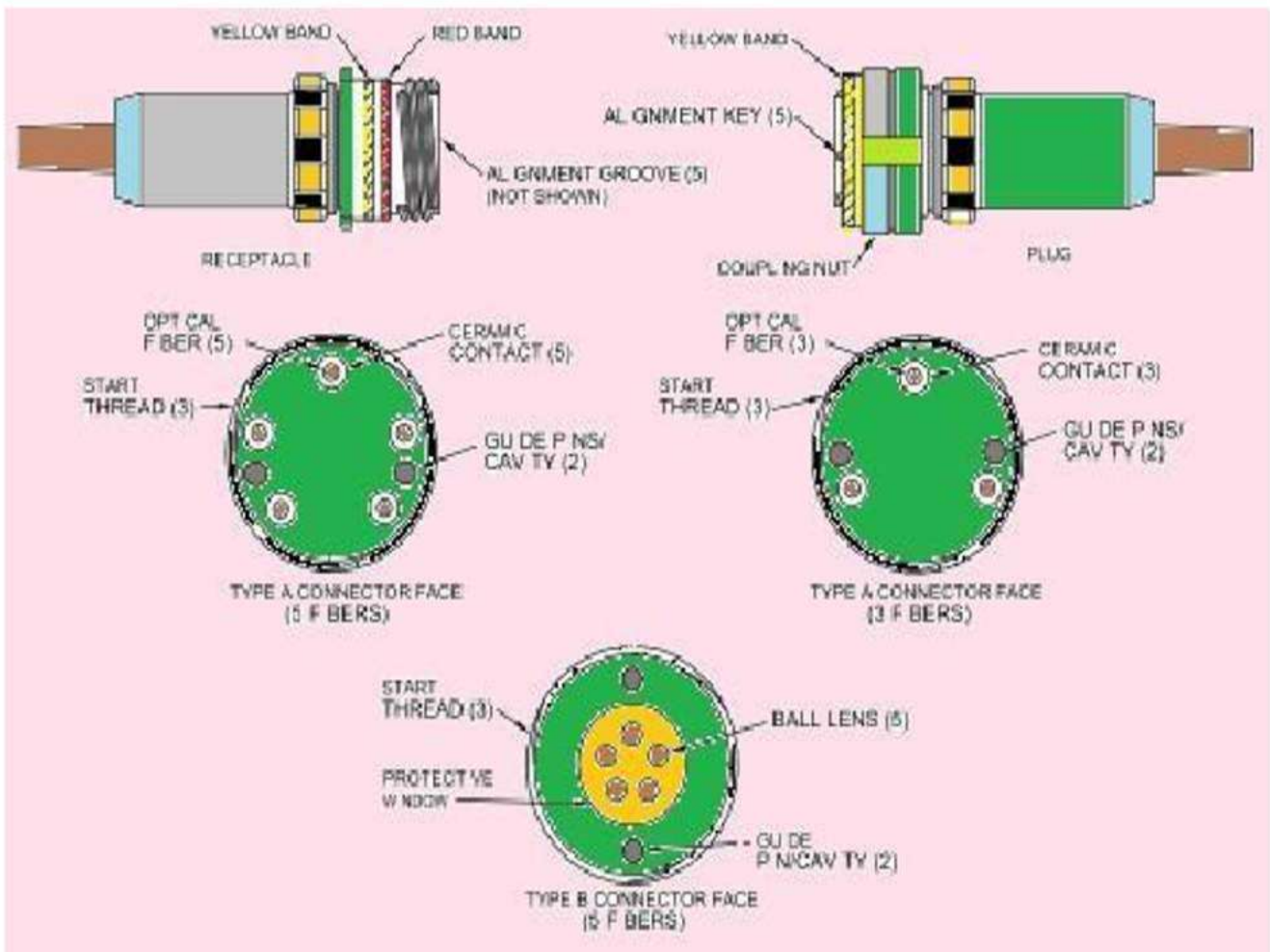
Figure 10.19: Types of Connector

These are used to accurately align the connector optical components; the guide pins in the plug fit into cavities in the receptacle when the plug and receptacle connect. In order to ensure that the connector is not over-tightened (which may cause damage to the fibers) the pins of the plug are designed to provide a buffer stop against the bottom of the cavities in the receptacle. The plug and receptacle have ceramic contacts that are designed to make physical contact when properly connected (the light signal passes through the through holes in the end of the ceramic contacts when they are in direct physical contact with each other).

The coupling nut on the plug barrel has a yellow band whilst the receptacle barrel has a red and a yellow band. A correct connection is made when the red band on the receptacle is at least 50 percent covered by the coupling nut. This position indicates an effective connection in which the optical fibers in the plug are aligned end-to-end with the fiber in the receptacle. Three start threads on the plug and receptacle ensure a straight start when they join. The recessed receptacle components prevent damage from the plug if it strikes the receptacle at an angle. The plug and receptacle are automatically sealed in order to prevent the ingress of moisture and dust.

FIBRE OPTICAL COMPONENTS

1. COUPLERS (WITH THREE OR FOUR PORTS)

If we want to connect many Transmitter to many receivers, we need to be able to distribute the optical signal and this is simply done by using a passive device, one that requires no power for its operation. Of course, such a device cannot increase the power of the signal—it can only decrease it. Fiber optic couplers are devices that split, combine or multiplex optical signals without added power. A (1 X N) splitter or tree coupler (Fig. 1), splits a single input into N equal channels or combines signals from N channels into one. A star coupler usually has equal umbers N of input and output ports (NXN). It may also have an unequal number of input and output ports (M X N). There are losses in couplers such as Split loss, Excess loss, Insertion loss, Back reflection, Directivity.
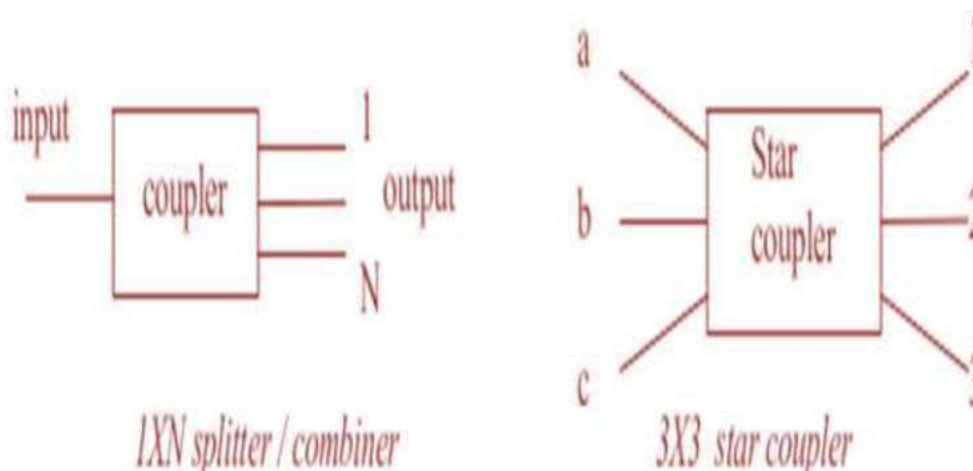
Figure 10.20

2. SWITCHES

(Using mirrors to deflect beams into different fiber strands)

3. ROUTERS

These devices are designed to control the routing of signals through the LAN and they comprise switches, processors, controllers, and one or more bus interfaces. The router processor sends control signals to the bypass switch unit (BSU). Typical BSU control signals are:
- PRI HI
- PRI RTN
- SEC HI
- SEC RTN

A logic high on PRI HI or SEC HI connects the BSU to the fiber optic ring. A logic low on PRI HI or SEC HI disconnects the BSU from the fiber optic ring. The PRI RTN and SEC RTN control signals are grounds (active low inputs) to the BSU switch relays. The fiber optic interface changes BSU fiber optic signals to electronic signals and electronic signals to BSU fiber optic signals.

TERMINATION OF A FIBER

There are various ways of handling fiber termination. The most common are: to prepare a fiber connector (for temporal fiber to fiber coupling), splice the fibers (for permanent coupling) or prepare high quality bare fiber tip facet (for e.g. Direct Source or detector coupling). In either case One needs to achieve a flat high quality facet surface, in order to avoid noticeable distortion of the wave front entering or exiting the fiber.

APPLICATION OF FIBER OPTIC IN AIRCRAFT

The Boeing 777 uses a fiber optic communications network called (Onboard Local Area Network) [shown in Figure-10.21]. These two fiber optical networks conform to the ARINC 636 standard which was adapted for avionics from the Fiber Distributed Interface (FDDI) in order to provide a network capable of supporting data rates of up to 100 Mbps. This is divided into two parts:
- Avionics local area network (LAN)
- Cabin LAN

The Avionics LAN connects the following LRU's:
- Left and right AIMS (Aircraft Information Management System).
- MAT (Maintenance Access Terminal).
- First Officers Side Display.
- Captains Side Display.
- B-Router.

The B-Router receives and sends signals to LRU's and connects signals to the P MATS (portable maintenance access terminals). The cabin LAN connects the following LRU's:
- ZNTU 1, 2, 3 (Zone Distribution Network).
- CFS (Cabin File Server)

5.11   ELECTRONIC DISPLAYS

In many ways, the Aircraft Electronic Displays may be made. The technology borrowed for aircraft's first instrument was from ships, railroad locomotives and auto-mobiles – transportation of the period. For simple parameters, dials and gauges were adequate. Even the first radio navigation instruments used simple pointer indicators for the Automatic Direction Finder and Course Deviation Indicator. In spite of the complexity, many aircraft are still full of mechanical displays. The ultimate navigation instrument, however, would be a map with the familiar "You are here" arrow. On the display is your flight plan, destination, location of bad weather, obstructions and collision hazards. This display depends on the ability to pictorially present information.

Other data can be displayed with numbers and letters, or alphanumeric. Examples are engine parameters, radio frequencies, airports, outside air temperature, airspeed and so on. Any parameter that is scalar can be shown with an alphanumeric display, while data that are vectors, such as courses, tracks, and headings, are best indicated with a graphic display. A reflective display (like a painted number) requires ambient light to be visible; it does not generate light. All mechanical pointer displays are reflective. For alphanumeric, numbers are painted on rotating drums mounted behind a window on a panel. The drum rotates and displays characters similar to the way a mechanical odometer operates in an automobile. The first DME's were made this way; with distance displayed on rotating drums. An early emissive display was the warning lamp. An example is a gear up – gear down light and a marker beacon indicator. One requirement of a warning light is high brightness; it must be seen in sunlight, which can be very bright in a cockpit.

There are no trees or clouds to shade the sun from an aircraft at high altitude. To reduce direct sunlight, a glare shield creates a "roof" at the top of the instrument panel. Even with this shield, emissive displays must be very bright. At the other end of the emissive brightness scale is the dark of night, where displays are reduced in intensity. There could also be a single warning light with so much illumination that night vision of the crew would be affected. (This is more critical in military flying than in the civil world.)

Principles Of Operation Of Display Technologies

INCANDESCENT

One of the first technologies in aircraft was the incandescent lamp, leading to the first alphanumeric electronic displays. The incandescent was probably the first application of the segmented numeric

display, where digits are formed by seven segments. Illumination comes from filaments stretched between posts (see Figure 11.1).
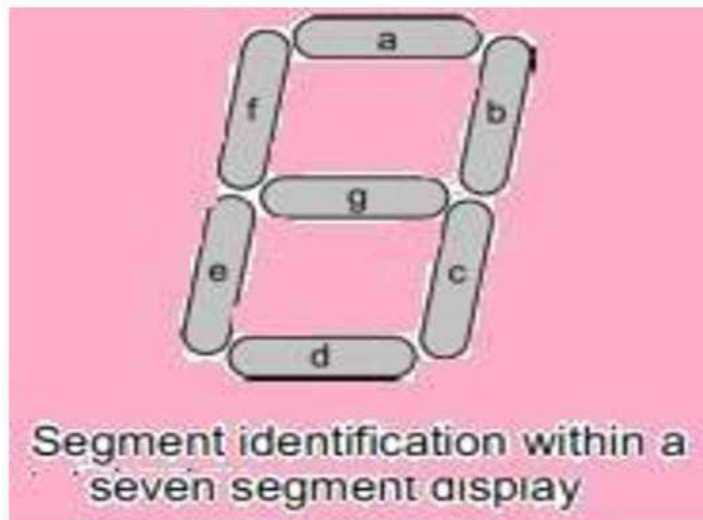
Figure 11.1: Seven Segment Incandescent Display

The display provides 10 decimal digits. Light emitted by the display is close to white. When intensity is reduced, the colour shifts to longer wavelengths and appears more orange. This was not a bad characteristic because redder light does not affect night vision as much as shorter wavelengths. Filters over a display can generate colors other than white. This is a problem, however, when the display is reduced in intensity and shifts toward red. Although the incandescent is still found in many aircraft, there are limitations. First, it is not suitable for alphanumeric displays. There are alphanumeric displays with 16 segments and numerals are acceptable. Letters of the alphabet, however, are difficult to read. Another problem is efficiency. At daytime brightness, the display becomes hot, limiting its life to approximately 5000 hours at moderate brightness. However, when the display operates at sunlight-readable intensity, life is reduced considerably. The final problem is cost. When incandescent displays became available, the high cost was acceptable since they were the only choice. Later technologies are much less costly.

PLASMA

A display technology used in significant numbers before LED's was introduced is plasma. It is based on orange light emitted from ionized neon gas. An example is shown in Figure11.2. Neon gas is contained between two flat glass plates. The rear glass is coated with a conductive material, usually a metal. Deposited on the inside of the front glass are metal segments. These can be a seven segment configuration or a customized pattern. The metal segments are very thin and transparent to light. If a sufficiently high electric potential is applied between the rear conductive coating and a metal segment, the neon gas ionizes. Orange light is emitted when neon atoms return to their zero energy state. By selectively energizing segments, numeric digits are generated.
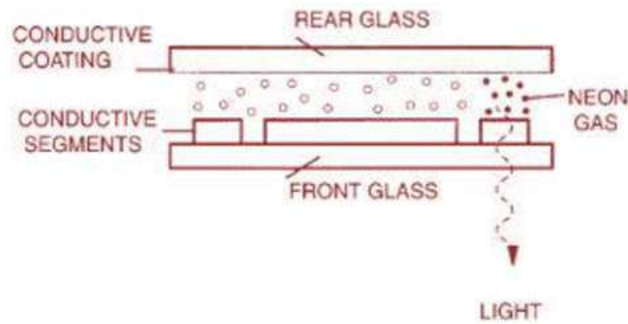
Figure 11.2: Plasma Display

CATHODE RAY TUBES (CRT)

Apart from mechanical indicators, filament lamps, and moving coil meters, the cathode ray tube is the oldest display technology in current aircraft use. Despite its age, the CRT offers a number of significant advantages, including the ability to provide an extremely bright colour display which can be viewed over a wide range of angles. For these two reasons, CRT displays are still found in modern aircraft despite the increasing trend to replace them with active matrix liquid crystal displays (AMLCD).

CONSTRUCTION

The internal arrangement of a typical cathode ray tube is shown in Figure 11.6. The cathode, heater, grid and anode assembly forms an electron gun which produces a beam of electrons that is focused on the rear phosphor coating of the screen. The heater raises the temperature of the cathode which is coated with thoriated tungsten (a material that readily emits electrons when heated). The negatively charged electrons form a cloud above the cathode (the electrons are literally 'boiled off' the cathode surface) and become attracted by the high positive potential that appears on the various anodes. The flow of electrons is controlled by the grid. This structure consists of a fine wire mesh through which the electrons must pass. The grid is made negative with respect to the cathode and this negative potential has the effect of repelling the electrons. By controlling the grid potential it is possible to vary the amount of electrons passing through the grid thus controlling intensity (or brightness) of the display on the screen. The focus anodes consist of two or three tubular structures through which the electron beam passes. By varying the relative potential on these anodes it is possible to bend and focus the beam in much the same way as a light beam can be bent and focused using a biconvex lens. The final anode consists of a graphite coating inside the CRT. This anode is given a very high positive potential (typically several kV) which has the effect of accelerating the beam of electrons as they travel towards it. The result is an electron beam of high energy impacting itself against the phosphor coating on the inside rear of the screen area. The energy liberated by the collision of the electrons with the phosphors is converted into light (the color of the light depending on the particular color of the phosphor at the point of impact).

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Internal arrangement of a CRT showing the path taken by the electron beam
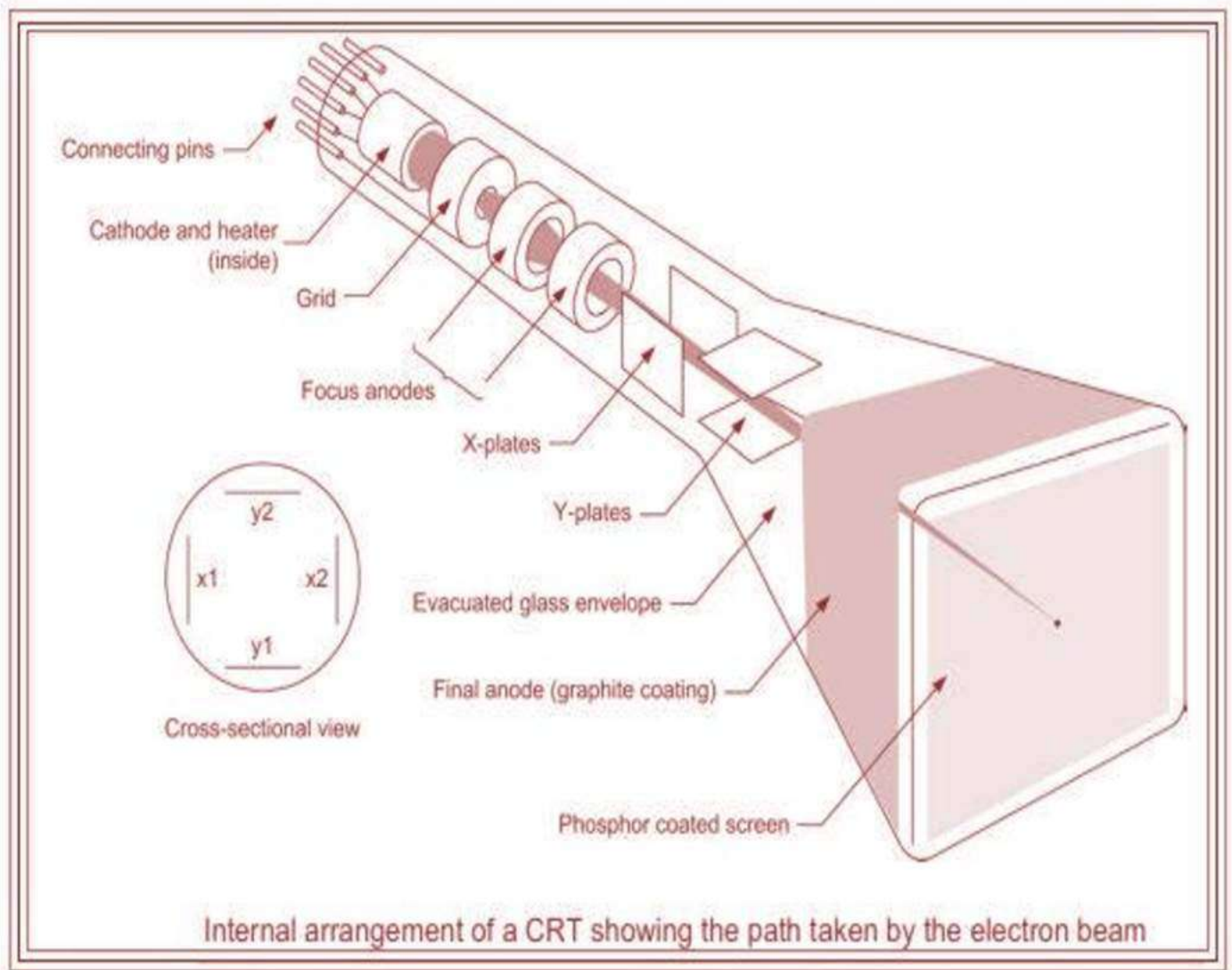
Figure 11.3

DEFLECTION

In order to move the beam of electrons to different parts of the screen (in other words, to be able to 'draw' on the screen) it is necessary to bend (or deflect) the beam. Two methods of Deflection are possible depending on the size and application for the CRT. The method shown in Figure 11.4 uses electrostatic deflection (commonly used for small CRT displays). Using this method two sets of plates are introduced into the neck of the CRT between the focus anodes and the final anode. One pair of plates is aligned with the vertical plane (these X-plates provide deflection of the electron beam in the horizontal direction) whilst the other pair of plates is aligned in the horizontal plane (these Y-plates provide deflection of the electron beam in the vertical plane). By placing an electric charge (voltage) on the plates it is possible to bend the beam towards or away from a particular plate
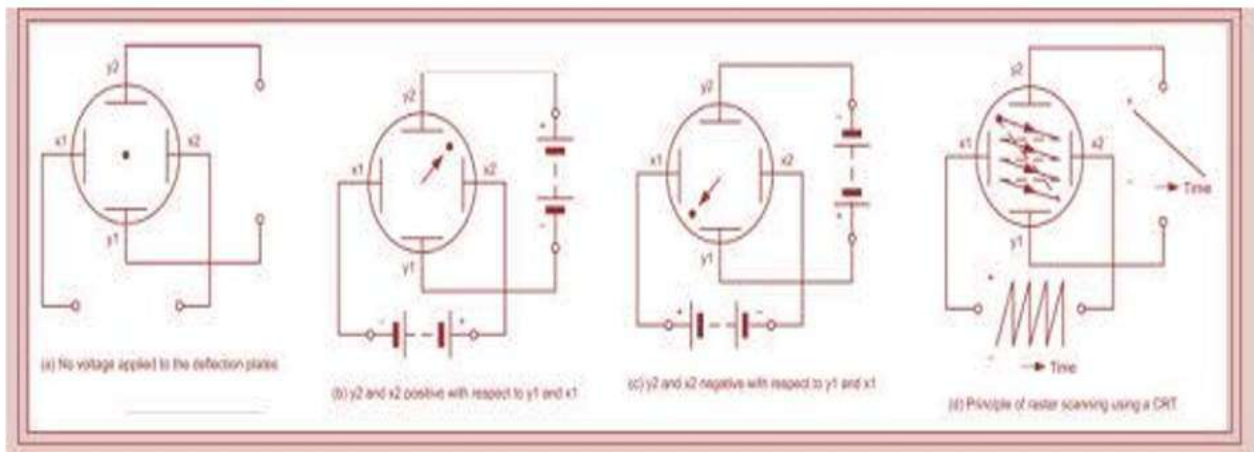
Figure 11.4: Deflecting the beam in a CRT using electrostatic deflection

SCANNING

In order to scan the full area of the CRT it is necessary to repeatedly scan the beam of electrons from top to bottom and left to right, as shown in Figure 11.7(d). The voltage waveforms required on the X and Y plates to produce the scanned raster must be ramp (sawtooth) shaped with different frequencies. For example, to produce the extremely crude four-line display shown in Figure 11.7 (d) the ramp waveform applied to the X-plates would be 50 Hz whilst that applied to the Y-plates would be 200 Hz. A complete raster would then be scanned in a time interval of 20 ms (one fiftieth of a second). A high resolution display will clearly require many more than just four lines however the principle remains the same. Suppose that we need to have 400 lines displayed and we are using a 100 Hz ramp for the Y-plates. The X-plates would then need to be supplied with a 40 kHz ramp waveform. Having produced a raster, we can illuminate individual picture cells (pixels) by modulating the brightness of the beam (we can do this by applying a 'video' signal voltage to the cathode of the CRT. Essentially, we are then modulating the beam of electrons with the information that we need to display. In effect, the electron beam is being rapidly switched on and off in order to illuminate the individual pixels. Text can easily be displayed by this method by arranging characters into a character cell matrix. Typical arrangements of character cells are shown in Figure 11.8. The alternative to electrostatic deflection is that of using an externally applied magnetic field to deflect the electron beam. This on method is known as electromagnetic deflection and it is based two sets of coils placed (externally) around the neck of the CRT. Comparable circuits of a CRT using electrostatic and electromagnetic deflection are shown in Figures 11.9 and 11.10 respectively

(a) 8 × 8 character cell   (b) 9 × 14 character cell

Examples of character cells
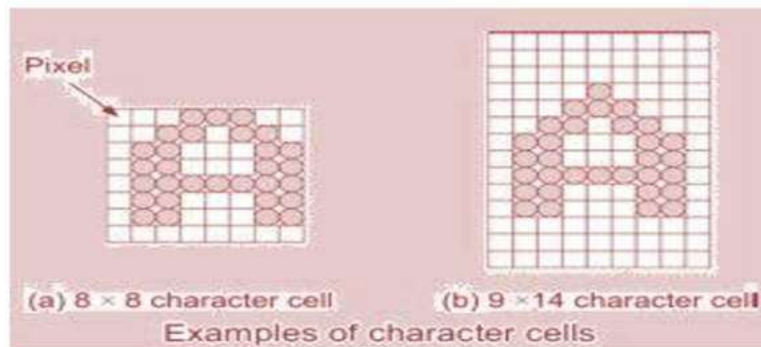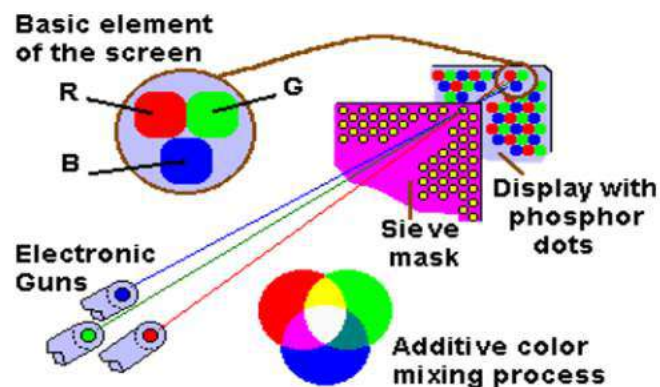
Figure11.5

Figure 11.6

CRT CONTROL

A dedicated CRT controller integrated circuit acting in conjunction with a video/synchronizing interface provides the necessary control signals for the CRT (including signals that are used to synchronize the X and Y-scanning ramp waveforms). In turn, the CRT controller acts under the control of a dedicated CPU which accepts data from the bus and buffers the data ready for display. Direct Memory Access (DMA) is used to minimize the burden on the CPU (which would otherwise need to process data on an individual byte or word basis). The patterns required to generate the displayed characters are stored in a dedicated character generator ROM. Data for each scan line is read out from this ROM and assembled into a serial stream of bits which are fed to the appropriate video signal channels.

ADVANTAGES OF THE CRT

- Full color graphics display
- Good resolution
- Sunlight readable
- Dimmable

- Reasonably power efficient
- Relatively inexpensive
- Wide temperature range
- Proven technology

DISADVANTAGES OF THE CRT

- Requires several power supply voltage***
- Requires very high voltage
- Generates magnetic fields which can radiate
- Is constructed with a fragile glass envelope
- Is heavier than other display technologies
- Requires significant depth behind the front panel

Item 5, (in disadvantages) on weight, includes magnetic deflection components and transformers for generating high voltage. Item 6 on panel depth is the most significant CRT problem. Depth represents wasted volume. Space behind the instrument panel is always tight in an aircraft and small assemblies are highly desirable. Most EFIS displays in aircraft currently used are CRT - based. The flat panel Active Matrix LCD however, is replacing the tubes in many existing and new-design aircraft.
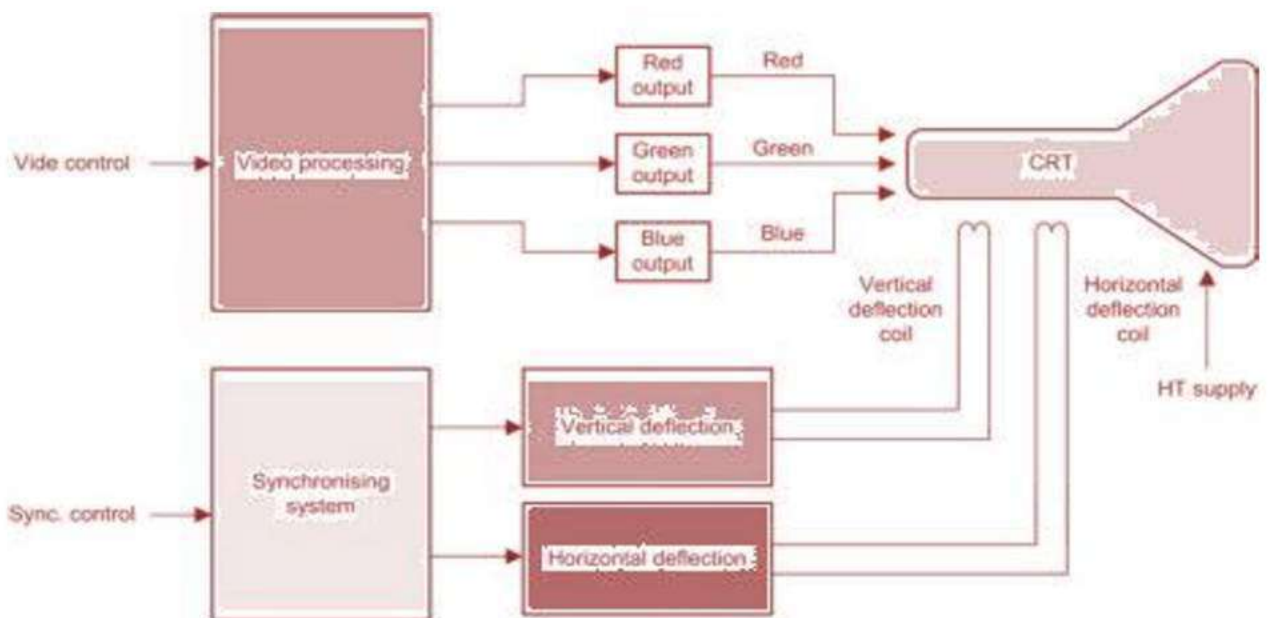
Arrangement of a colour display

Figure 11.7

LIGHT EMITTING DIODES (LED)

Light emitting diodes (LED) can be used as general-purpose indicators. When compared with conventional filament lamps they operate from significantly smaller voltages and currents. LEDs are also very much more reliable than filament lamps. Most LEDs will provide a reasonable level of light output when a forward current of between 5 mA and 20 mA is applied.

Table 11.1 Characteristics of various types of LED

Parameter	Type of LED			
	Miniature	Standard	High efficiency	High intensity
Diameter (mm)	3	5	5	5
Max. forward current (mA)	40	30	30	30
Typical forward current (mA)	12	10	7	10
Typical forward voltage drop (V)	2.1	2.0	1.8	2.2
Max. reverse voltage (V)	5	3	5	5
Max. power dissipation (mW)	150	100	27	135
Peak wavelength (nm)	690	635	635	635

Table 11.1

Light emitting diodes are available in various formats with the round types being most popular. Round LEDs are commonly available in the 3 mm and 5 mm (0.2 inch) diameter plastic packages and also in a 5 mm × 2 mm rectangular format. The viewing angle for round LEDs tends to be in the region of 20° to 40°, whereas for rectangular types this is increased to around 100°. Table 11.1 shows the characteristics of some common types of LED.

SPECTRAL RESPONSE

Light of different colors can be produced by using different semiconductor materials in the construction of an LED. However, there is a wide variation in both the efficiency and light output of LED of different colors. For this reason, red displays tend to be most common (with a peak output at around 650 nm). Note that this is towards one end of the visible spectrum, as shown in Figure 11.8.
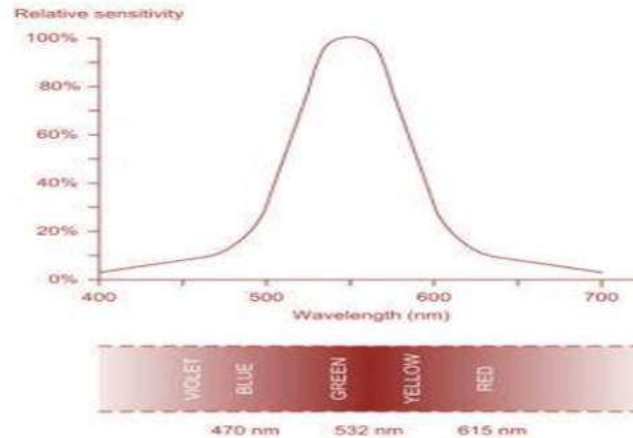
Figure 11.8

Figure 11.9: Typical example of a four-digit seven segment display

SEVEN SEGMENT DISPLAYS

LED displays are frequently used to display numerical data. The basis of such displays is the seven segment indicator (Fig. 11.15) which is often used in groups of between three and five digits to form a complete display. The arrangement of the individual segments of a seven segment indicator is shown in Figure 11.1 in the beginning. The segments are distinguished by the letters, a to
g. Since each segment comprises an individual LED it is necessary to use logic to decode binary (or binary coded decimal) data in order to illuminate the correct combination of segments to display a particular digit. For example, the number '1' can be displayed by simultaneously illuminating segments b and c whilst the number '2' requires that segments a, b, g, e, and d should be illuminated. The circuit of a seven segment display is shown in Figure 11.16 whilst a typical decoder and decoder truth table are shown in Figures 11.17 and 11.18 respectively.
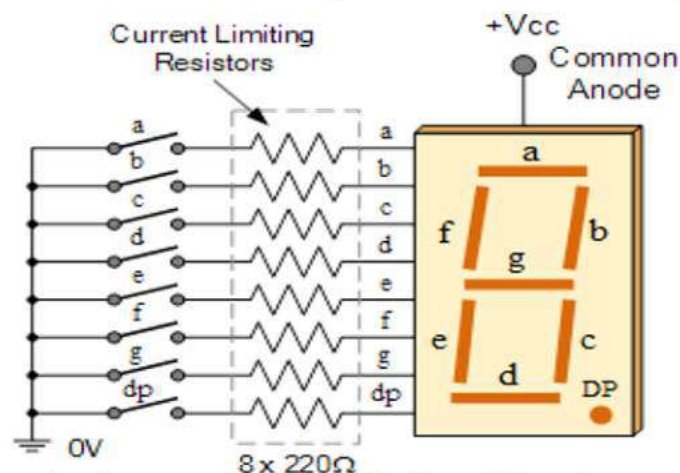
Figure 11.10. : Circuit of a Seven segment display with series current limiting Resistors
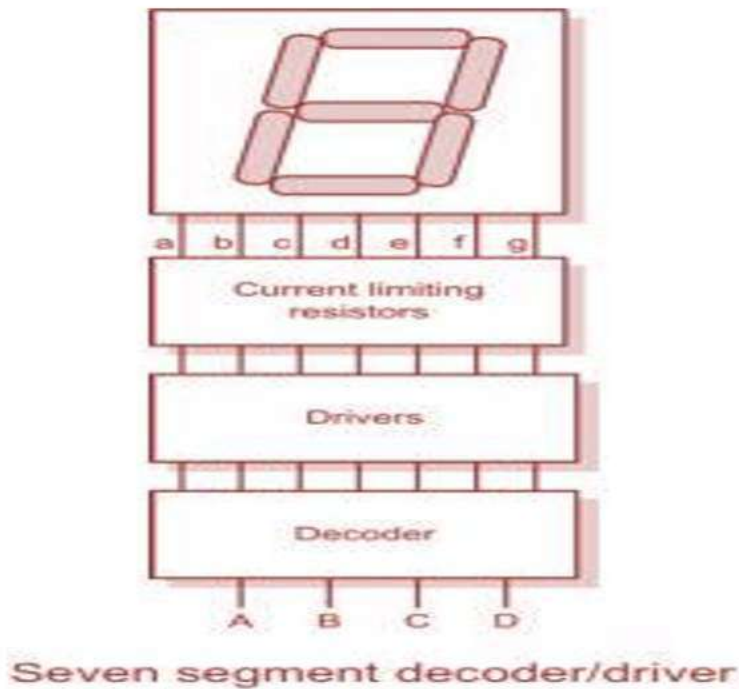
Seven segment decoder/driver

Figure 11.11

Figure 11.12 : Truth table for the decoded seven segment display

LIQUID CRYSTAL DISPLAYS (LCD)

Liquid crystals have properties that can be considered to be somewhere between those of a solid and those of a liquid. Solids have a rigid molecular structure whilst the molecules in liquids change their orientation and are able to move. A particular property of liquid crystals that makes them attractive for use as the basis of electronic displays is that the orientation of molecules (and consequently the passage of light through the crystal) can be controlled by the application of an electric field. The newest technology goes toward improvement of the display units in the cockpit. These LCD units are smaller, lighter and use less power. There is no Radiation of electric or magnetic fields who must be shielded. The display has a better readability in bright sunlight and a very high resolution, so more information is displayable. As a safety aspect, there is no CRT to implode and no more very high voltage are used. The reliability is high; there are no adjustments for purity, convergence, focus and deflection necessary. The cost of a LCD is higher than of a CRT, because it is more difficult to

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manufacture it. The chance to have failed picture elements (pixels) is high, with so many active transistor-elements. The DU contains a display glass assembly with liquid crystal display LCD elements. About 4 million thin film transistors (TFT) absorbing or conducting the light from the bright backlight assembly through the glass panel. Each color dot has 3 transistor elements. One for red, green and blue to produce the desired color.

TYPES OF LCD

LCD displays can be either reflective or backlit according to whether the display uses incident light or contains its own light source. Figure 11.13 (a), (b) and (c) shows the construction of both types of display. Note that, unlike LED, liquid crystal displays emit no light of their own and, as a consequence, they need a light source in order to operate.
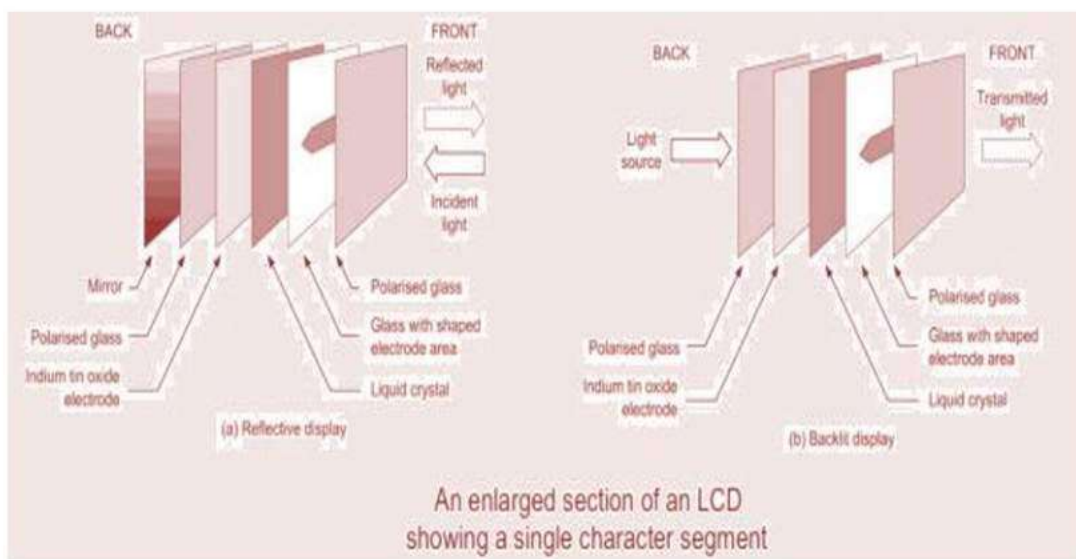
Figure 11.13(a)
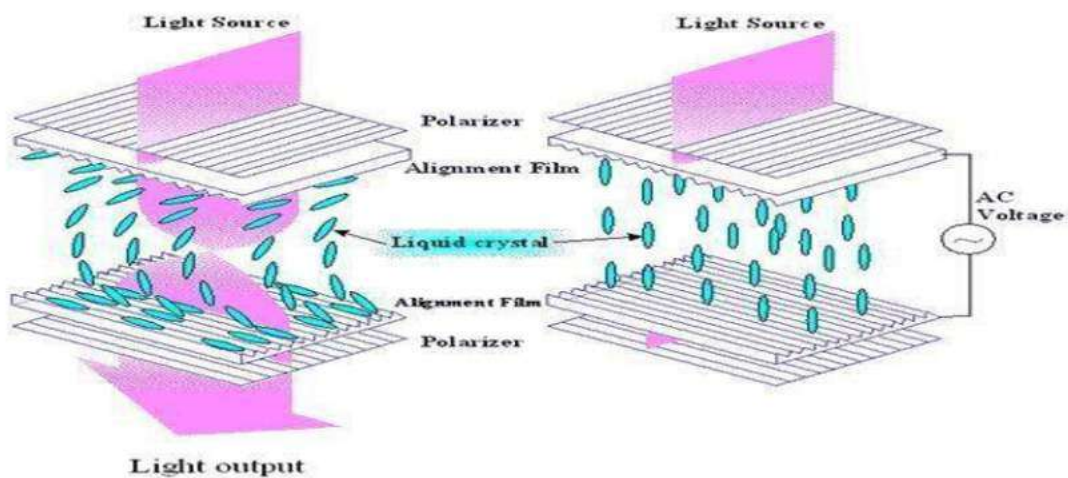
Figure 11.13(b)
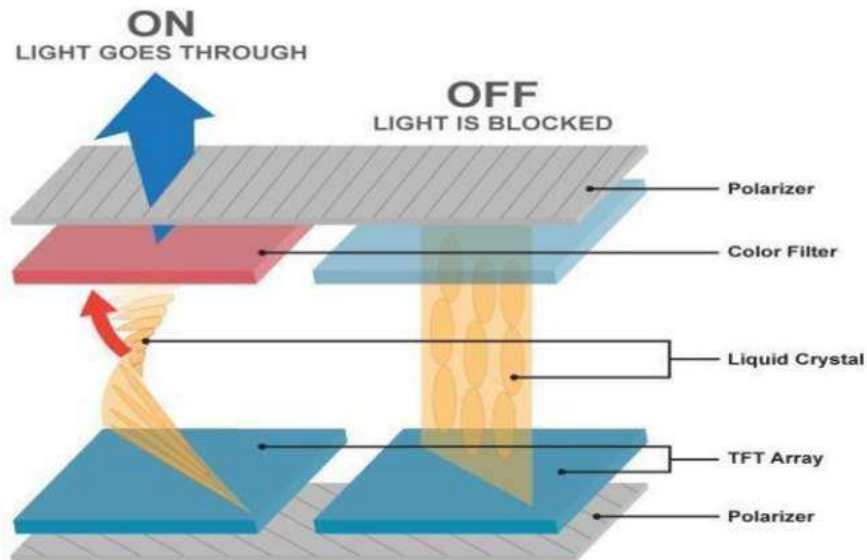
Figure 11.13(c)

Larger displays can be easily made that combine several digits into a single display. This makes it possible to have integrated displays where several sets of information are shown on a common display panel.

PASSIVE MATRIX DISPLAYS

In order to display more detail (for example, text and graphics characters) LCD displays can be built using a matrix of rows and columns in order to produce a display that consists of a rectangular matrix of cells. The electrodes used in this type of display consist of rows and columns of horizontal and vertical conductors respectively. The rows and columns can be separately addressed (in a similar manner to that used for a memory cell matrix, see page 67) and individual display cells can thus be illuminated. Passive matrix displays have a number of disadvantages notably that they have a relatively slow response time and the fact that the display is not as sharp (in terms of resolution) as that which can be obtained from an active matrix display.

ACTIVE MATRIX DISPLAYS

Active matrix LCD (AMLCD) use thin film transistors (TFT) fabricated on a glass substrate to that they are an integral part of a display. Each transistor acts as a switch that transfers charge to an individual display element. The transistors are addressed on a row / column basis as with the passive matrix display. By controlling the switching, it is possible to transfer precise amounts of charge into the display and thus exert a wide range of control over the light that is transmitted through it. Color AMLCD comprise a matrix of pixels hat correspond to three colors; red, green and blue. By precise application of charges to the appropriate pixels itis possible to produce displays that have 256 shades of red, green and blue (making a total of more than 16 million colors). High resolution color AMLCD make it possible to have aircraft displays with a full graphics capability.

ELECTRONIC BOARDS

REAR CONNECTOR

MOTHERBOARD

BACKLIGHT ASSEMBLY

LIQUID CRISTAL DISPLAY
GLASS ASSEMBLY

LIGHT SENSOR

Example of an Active Matrix *LCD* Display Unit
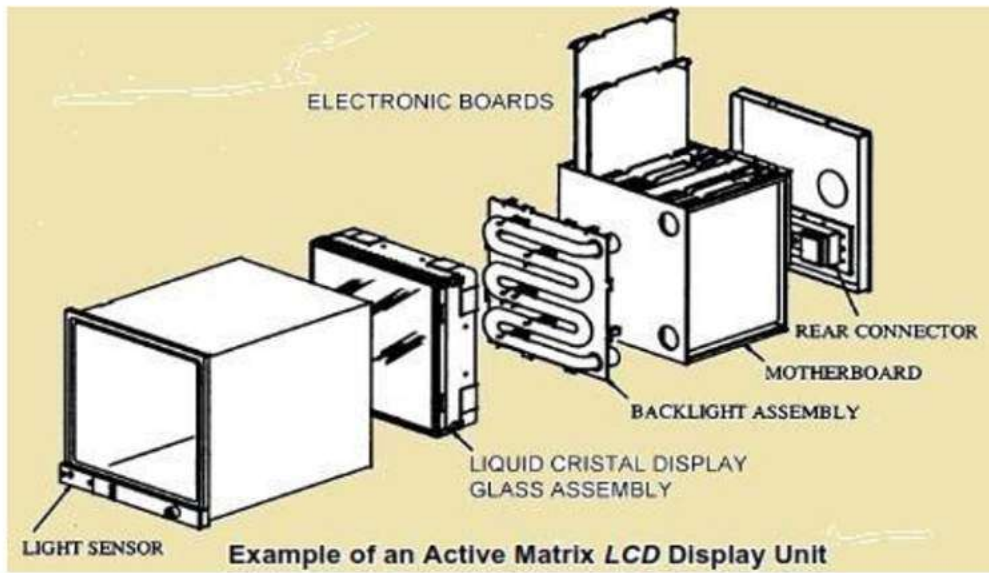
Figure 11.14

5.12 ELECTROSTATIC SENSITIVE DEVICES

INTRODUCTION

Electrostatic discharge is defined as the transfer of charge between bodies at different electrical potentials. The electrostatic discharge occurs when two different materials rub or slide together or are separated. Examples are: walking over synthetic floors, rubbing of synthetic garments, shifting of plastic boxes, unrolling of PVC adhesive tape, moving of convey or belt. (Figure 12.1)
When two objects with different charges get closer, electrons can suddenly flow from one object to the other insulators are common plastics, glass and air.

CAUSE OF STATIC ELECTRICITY POSITIVE AND NEGATIVE CHARGES

- Whether or not an item becomes subject to 'positive' or negative' electrostatic charges stems from the atomic or molecular structure of the materials involved in its manufacture. Materials which will readily give up electrons become charged positively, whereas others which have an affinity for electrons become charged negatively. Whenever two items are brought into contact and then separated, there is likely to be electron transfer and thus electrostatic charging, which can result both from rubbing or non-frictional contact/separation. The net charges on the two materials will be equal but the conductivity (or resistivity) of the materials will greatly affect the potential electrostatic charges involved.

- The charges tend to dissipate quickly over the entire surface of conductive materials, which not only lowers the electrostatic potential but increases the possibility of further dissipation to other materials which are in contact directly or via an air space.

- On non-conductive materials the electrostatic charge can remain in localized areas at high potentials, creating electrical fields between themselves and other materials at different potentials and ground. Materials entering these fields can be charged by induction, which takes place when electrons of the material entering the field are attracted to those areas closest to any one of positive potential, leaving behind positive charged areas and creating negative charged areas.
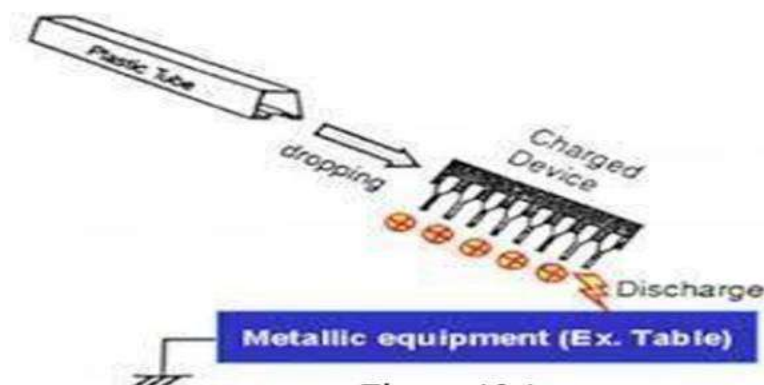
Figure 12.1

TRIBOELECTRIC EFFECT

- When two dissimilar non-conducting materials are rubbed together, the friction transfers electrical charge from one material to the other. This raises the electrical potential between the materials, and is known as the triboelectric effect. The build-up of charge, and subsequent attraction of materials, can be observed when film is separated from its roll. The polarity and strength of the electrical charges depend primarily on the materials, surface finish, ambient temperature and humidity. The Triboelectric series classifies different materials according to how readily they create static electricity when rubbed with another material. The series is arranged on a triboelectric scale of increasingly positive and increasingly negative materials. Materials that give up electrons and become positive when charged (thereby appearing as positive on the triboelectric scale) include:

- Glass

- air and

- dry human skin.

Materials that attract electrons become negatively charged (appearing as negative on the triboelectric scale) include:

- Polyester
- Polystyrene
- Polyethylene
- Poly (Vinyl Chloride) (PVC).

PRIME ELECTROSTATIC GENERATORS

Materials common to electronic maintenance, repair and testing, which can be factors in the generation of electrostatic charges, include the human body, all work surfaces, floors (especially if waxed), furniture, personal clothing (including clean room garments), tools and all non-conductive packaging materials. Some type of motion is required for the generation of electrostatic charges and some non-conductive materials are extremely good generators of such charges. Nylon shirts or smocks, for example, can easily become charged to 20 000 V or higher.

- The human body is, in all likelihood, the most frequent source of damage to sensitive electronic components as a result of electrostatic discharge. The electrostatic potential of the human body is a function of many variables, such as body capacitance, clothing material and style, body activity, relative humidity of the air, footwear, etc. A widely accepted electrical model for the human body is a capacitor (CHB) and a series resistor (RHB). There must, obviously, be a wide range of published values for both parameters, as many variables can affect them, e.g. body size, muscle tone, skin ruptures (spots, cuts, etc.), skin moistness, contact area, footwear, position in relation to the work piece, etc. However, the consensus of

opinion would appear to support 200 pF as a reasonable approximation for CHB and 1000 ohms for RHB

SPECIAL HANDLING OF COMPONENTS SENSITIVE TO ELECTROSTATIC DISCHARGES

MATERIALS

1. SHIELDING MATERIALS

These materials provide a Faraday cage protection, limit the passage of current and attenuate the energy resulting from an electrostatic discharge. Most static shielding materials include a conductive metal or carbon element that suppresses the field, attenuates, or reflects field energy.

2. CONDUCTIVE MATERIALS

These materials characterized by a low electrical resistance and allow the charge to quickly distribute itself throughout the material. If the conductive material is connected to ground, all charge will flow away. Some examples of conductors are metals, carbon and the human body's sweat layer.

3. STATIC - DISSIPATIVE MATERIALS

In these materials Charges will flow to ground slower than with conductive materials, reducing its destroying potential.

4. INSULATIVE MATERIALS

Are those having high electrical resistance and are difficult to ground. Static charges remain in place on these materials for a very long time. This property make insulators a hazard that must be controlled as part of an ESD program.

AWARENESS OF RISKS AND POSSIBLE DAMAGE, COMPONENT AND PERSONNEL ANTI-STATIC PROTECTION DEVICES.

DEVICES SUSCEPTIBLE TO ELECTROSTATIC CHARGE

Certain semi-conductor devices are susceptible to damage from electrostatic charges and are at risk in any environment where they may come into contact with such charges. The prime risk during maintenance activities is the static charge held on personnel and tools, whilst in storage the risk is from the charge held on personnel and non-conductive packaging materials. The devices which are susceptible to electrostatic charge are:

- The metal oxide semi-conductor (MOS) and complementary MOS (CMOS) family of devices .Discrete transistors and diodes, Field Effect Transistors (FET) and Schottky TTL devices also suffer damage from electrostatic discharges.
- Bi-polar devices. Operational Amplifiers, Emitter-coupled Logic (ECL) devices and Transistor-transistor Logic (TTL) devices.
- In addition, thin film resistors, multi metal-layer hybrid substrates.

Device Type	ESD Susceptibility
CMOS	250 - 3000 Volt
OP-AMP	190 - 2500 Volt
VMOS	30 - 1800 Volt
MOSFET	100 - 200 Volt
GaAsFET	100 - 300 Volt
EPROM	100 Volt
JFET	140 - 7000 Volt
BI-POLAR TRANSISTOR	380 - 7000 Volt
SCHOTTKY DIODES	300 - 2500 Volt
SCHOTTKY TTL	1000 - 2500 Volt

Table- 12.1, shows the ESD for various type of Semiconductor devices.

ESD DAMAGE

It can occur at any time such as GOODS INPUT, ACCEPATANCE, PRODUCTION, ASSEMBLY, TESTING, STORING, PACKING, SHIPPING, MAINTENANCE.

CONTROL

Basic ESD controls is by GROUNDING, SHIELDING, NEUTRALIZATION (Ionizers).

GOLD RULES

- Assume that all active components are sensitive to ESD.
- Handle electronic components only in the ESD protected area (EPA) and only when you are properly grounded.
- Store and transport the ESD-sensitive items in ESD protective containers.
- Check regularly the ESD protection system, internal and external (suppliers).
- All equipment must be free of moving parts that may generate charges, e.g., rubber rollers, plastic stoppers, etc.
- Things which the devices may come in contact with or get transported on must also be antistatic or conductive.
- The minimization of movements in the work area, as well the use of ESD-safe equipment, will help in minimizing static charges generated by personnel.

ESD ELIMINATION

The heart of an ESD control program is the ESD-protected work area and ESD grounded work station. When you handle an ESD- sensitive device outside of its ESD protective packaging, you need to provide a means to reduce generated electrostatic voltages below the levels at which the item is sensitive. The greater the margin between the level at which the

generated voltages are limited and the ESDS item sensitivity level, the greater the probability of protecting that item.

EPA AREA

An EPA (ESD Protected Area) is a defined space where no items or activity are able to cause damage to a sensitive device. In the simplest case - a field work station - it may consist of a dissipative mat, a wrist strap and common grounding facility for both. [Figure-12.2]

Figure 12.2 EPA
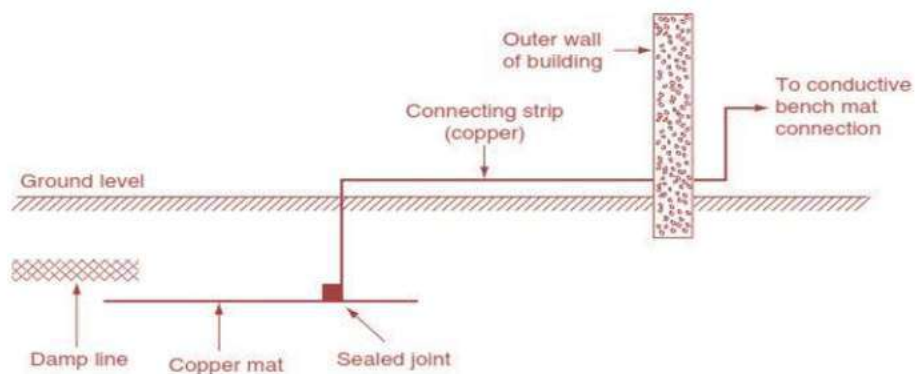
Figure 12.3: ESD Work Area Protection

PERSONNEL ESDS DEVICES

- WRIST-STRAP

The wrist strap is the most used device to ground personnel; it will safely and effectively drain static charges from the body. The wrist strap with coiled cord should have resistance of the order of at least $1 M\Omega$.

- FOOTWEAR

In some locations, such as stores and around equipment, conductive shoes or foot grounders are used. Foot grounders should be worn on both feet to ensure constant contact to ground floor or

floor mat. Foot grounders will not function properly if used on surfaces which are insulative or improperly grounded. (As shown in Figure 12.5).

- GARMENTS

The main purpose for wearing conductive smocks is to suppress static fields on employee clothing. The conductive fibers woven into the material provide a Faraday cage that prevents dangerous fields from extending to and damaging sensitive products. There shall be electrical conductivity between all parts of the garment.

- GLOVES

ESD sensitive device can experience a damaging discharge if touched by a person, even if that person is properly grounded. Increasing the electrical path's contact resistance is one way to control the speed of the discharge. A good way to accomplish this is by wearing static dissipative cots and gloves.

- CHAIRS

At least two castors or feet must provide a path to ground.

Figure 12.4

ELECTROSTATIC-FREE WORK STATION

Things to be considered to set up an electrostatic-free work station.

1. HUMIDITY
A factor which needs to be considered when working with electrostatic-sensitive devices is the humidity of the working environment. The air in a very low-humidity environment is dry and has a very high resistance, such air will not discharge the static electricity as quickly as a moist air. Therefore, the working environment for an electrostatic-free work station should ideally, have a relative humidity of between 30 and 50%.

2. WORKING ENVIRONMENT
There are two basic methods of achieving a safe working environment:
- Conductive work surface and tools in use should be bonded electrically to a common ground.
- Make an ionised atmosphere to dissipate static electrical charges

3. GENERAL OPERATING PROCEDURES

CONDUCTIVE-SURFACE WORK STATION

Following should be checked for an effective ground and periodically monitored thereafter.

- In order to establish that wrist straps have not developed any faults, periodic checks should be made on their resistive valuei.e. $1M\Omega$.
- Under no circumstances should the operator, or anybody else, touch electrostatic sensitive devices, or assemblies containing such devices, without first having placed a wrist strap indirect contact with their wrist.

- When a conductive surface station is equipped with an air- ioniser blower, the normal operating procedure is to allow the blower to operate for approximately two to three minutes before performing any work. The operator should also move their hands into the ionised airstream for a few seconds, to allow for charge dissipation, before handling electrostatic-sensitive devices.
- The effectiveness of an electrostatic-free work station can be further checked by the use of an electrostatic-detecting meter. Such meters are normally capable of detecting the presence, indicating the polarity and level of static electricity and can be read on various scales, ranging from 30 to 50000 V at distances of 6.5 to 30 cm (2.5 to 12 in).

GENERAL HANDLING PROCEDURES

It is not possible to lay down a degree of electrostatic protection which would cover all types of semi-conductor. However, there is a strong consensus of opinion that a significant reduction of dangers related to electrostatic charges can be achieved by making personnel aware of possible electrostatic generators and improved general handling techniques, such as:

- Use conductive packaging, shorting plugs, bands or wire when provided or prescribed in the relevant aircraft or equipment Maintenance Manual.
- Not unnecessarily touching the connectors, leads or edge connectors, etc., of printed circuit boards containing such devices.
- For both serviceable and unserviceable electrostatic-sensitive devices, modules and printed circuit boards the same precautions should be observed.
- Persons engaged in maintenance or repair work should be electrostatic conscious and should consider the avoidance of damage by electrostatic charges as a normal responsibility. They should also be aware of the necessity for the elimination of electrostatic generation such as plastics envelopes, non- conductive tapes and other commonly used items made from plastics, nylon and rubber.
- The effectiveness of an electrostatic-free work station should be regularly checked with a static-detecting meter.

- Work which involves the handling of exposed electrostatic- sensitive devices should not normally be undertaken outside the confines of an electrostatic-free work station. 4 Soldering irons should always be used with a grounded bit.
- Any accumulated electrostatic charge on other hand tools should be discharged prior to the tool being used.
- It is, advisable to retain any conductive or anti-electrostatic packaging material removed from serviceable equipment for re-packaging of the unserviceable items. Ensuring that the package is suitably labeled to show that the contents are unserviceable but contain electrostatic-sensitive devices.

TESTING

GENERAL

All testing of equipment containing electrostatic-sensitive devices should be strictly in accordance with the relevant manufacturer's instructions. The following explanation only draw attention to the more general precautions which should be observed during testing of electrostatic-sensitive devices and/or printed circuit boards or modules.

- In general, such, items should not be inserted or removed from their installed positions unless all electrical power is switched off, as transient voltages may cause permanent damage.
- When bench testing, input test signals should not normally be injected into such items without electrical power being applied. All unused input connections should also, normally, be connected to a power source or to ground.
- Much of the test equipment used for the testing of such items will also contain electrostatic-sensitive devices. While calibration of this type of test equipment will not normally require the operator to wear a wrist strap, if a repair or replacement has to be made involving an exposed device or module, then a wrist strap should be worn and the electrostatic damage-prevention measures mentioned here to be followed.

STORAGE

- It is known that plastics and polymer based packaging materials will retain static charges which produce voltage gradients across the surfaces; accordingly, electrostatic- sensitive equipment must never be stored alongside non- electrostatic sensitive equipment.
- Electrostatic-sensitive equipment should be packed in a conductive material, such as will ensure that the whole of the package is maintained at the same potential and should then be stored in grounded metal racks or cupboard

BASIC SYMBOL

The basic symbol consists of a yellow hand within a black triangle. It is intended to identify devices and assemblies which are ESD sensitive.
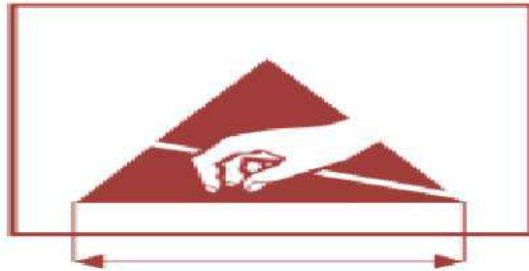
Figure 12.5

PROTECTION SYMBOL

Used to designate all ESD protective products such as bags, boxes, garments. A letter is added under the symbol to indicate the primary function:

Figure 12.6

EPA SYMBOL

Used to designate EPA equipments such as tables, trolleys, chairs.

Figure 12.7

EPA CAUTIONARY SYMBOL
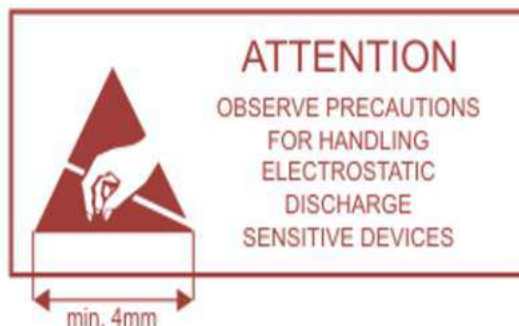
Figure 12.8

EARTH BONDING POINT (EBP)

Figure 12.9

ESD PROTECTED AREA (EPA)

Figure 12.10

HIGH VOLTAGE ESD PROTECTED AREA (EPA)

Figure 12.11

5.13 SOFTWARE MANAGEMENT CONTROL

Many modern aircraft have systems that are operated or controlled by software. This software is developed and approved under the relevant certification processes. Since the operation and functionality of systems is controlled by software, that software is an integral part of the system and is covered by any approval the product or appliance may have. A feature of aircraft system software is that it is usually quite easy to change the software loaded into a system.

Changing the software loaded into a system does not make any visual change to the equipment and in many cases does not cause the hardware part number on the equipment to change. The component parts of modern aircraft systems often require a specific software configuration to allow the system to function correctly. Thus it is important that the software installed in aircraft systems is maintained in a configuration relevant to that particular aircraft. In aircraft fleets, it is common for system changes to cut in at a particular aircraft or equipment serial number.

This means that different software configurations are required for different aircraft in the fleet. In modern aircraft, particularly the more complex types, software provides functions that are critical to the safe operation of the aircraft. With the considerable use of software on modern aircraft used in essential systems such as flight controls, engine controls, electrical generation, navigation flight instruments and auto-flight it is essential that the software design must be investigated and control of its certification maintained. The basis for the certification of software in aircraft equipment and systems is RTCA (Radio Technical Commission for Aeronautics) document DO-178B, and EUROCAE (European Organization For Civil Aviation Equipment) document ED-12/ 12B entitled "Software Considerations in Airborne Systems and Equipment Certification". Each digital LRU (Line Replaceable Unit) consists of Hardware, the electronic devices, and Software, instructions that tell a computer what to do. Software comprises the entire set of programs, procedures, and routines associated with the operation of a computer system.

With the ease with which software can be loaded into systems, it is essential that all operators with aircraft that utilize software manage the configuration. If the software configuration is not managed, it is quite possible for systems to not operate efficiently or to have significant malfunctions. Changing the software configuration in a system is a design change except when the change is to an aeronautical database. Thus the software configuration is an inherent part of the overall configuration management of an aircraft. Since software is often changed, the conventional means of configuration management using the Illustrated Parts Catalogue or other equivalent means become impracticable. This is certainly the case where the software installed in a system component can be revised without removing the component from the aircraft. Thus the need has arisen for the configuration of the software loaded into system components to be managed at the

aircraft level rather than at the component level to ensure compatibility between systems and ensure continued compliance with airworthiness requirements.

SOFTWARE CONTROL LIBRARY

Concept A Software Control Library (SCL) can be developed as a physical location in which all master software versions are stored. The SCL may be used to maintain the configuration control of software. The SCL stores and categorizes software on different media. The master media is used to create copies of software images for the purpose of loading software on the aircraft. The SCL should have management procedures in place to ensure the integrity of the master software. The SCL can be in the form of an electronic library on a file server which is the preferred method of control of software distribution. The file server should have the capability to maintain software configuration. FLS can be managed in an operator's inventory system without creation of a SCL.

SOFTWARE DOCUMENTATION

Proper documentation should accompany Software (FLS) received from any supplier. Generally, an acceptable Authorized Release Certificate e.g. FAA Form 8130-3, EASA Form One, should accompany LSAP aircraft parts. If the FLS is received without adequate documentation, the operator must take all practicable steps to determine the airworthiness approval status of the software. The software supplier should provide appropriate conformity documents with the delivered FLS.

SOFTWARE CATEGORIES

LRU's of new generation often contains their software in different packages, which can be divided into different categories, Core Software or System Software, Operational Software or Application Software and Data Base Software. The Core Software refers to the operating system and all utility programs that manage computer resources at a low level. It also defines the interface of this specific LRU to other LRU's. The Operational Software, or Application Software, defines the part of a computer program that varies for different aircraft configuration or changes for each different airline. By implementing a new Data Base Software, only parameter values will be changed. Therefore it is not a program change. An example would be the navigation data base that contains flight plan information such as runway direction or landing system frequency etc. [Figure-13.1].
In the RTCA Document DO 178B, software levels are defined from A down to E

1. Level A, where anomalous behavior can cause a catastrophic result.
2. Level E, where anomalous behavior will not affect the safety of the aircraft.

STORAGE, TRANSPORTATION AND HANDLING

Subject to the availability of suitable loading capability on the aircraft, software may be stored on various types of media, including but not limited to the following media types; Floppy Disc, CDROM, DVD, PC Card. High density media sets are now being used for software to be stored and transferred. Multiple software programs or databases may be stored on one medium. Media handling practices should be developed based on recommendations from manufacturers of the media. Consideration should be given to avoid physical damage to the media due to factors such as temperature, humidity, vibration, electromagnetic radiation, dust, chemical and airborne contamination, moisture, and abusive handling. Transportation of Media Magnetic media that is transported from one location to another should be wrapped or bagged in a dust free, lint free, electrostatic discharge (ESD) protected material. In addition, media shipped to off-site locations should be packaged in a closed box or envelope. All media should be clearly and properly labelled for transport; all information on labels should be typed, stamped, machine printed or clearly hand-written. Media labelling is further defined in ARINC Report 665. Packaging should be clearly labelled as containing magnetic media, if applicable. Depending on the Software Level, different care must be taken in documentation and handling of the software. Only authorized personal may modify the software which is classified in level A. Software which is classified in level E can be done by maintenance personal, but only if respective documentation is available.

In any case it must be guaranteed that only the authorized software will be influenced by the load-activity, the successful loading must be acknowledged, no other systems will be affected. The Core-Software should normally never be touched, because it is a part of the control loop of the aircraft. An uncontrolled change could have a catastrophic effect on the aircraft. A change of this software can only be made with the agreement of the aircraft manufacture and the LRU manufacture. This is documented in authorized Service Bulletin (Cover-S/B) of this two manufactures. A change of the Operational/Application-Software needs also the agreement and documentation of both manufactures. But the LRU-Manufacture can be bypassed, if the airline engineering guarantees an 'equivalent-level-of-safety', a very complicate act. A Data Base Software change can normally be done without activity of the manufactures and if it is guaranteed that the software is classified in level E.
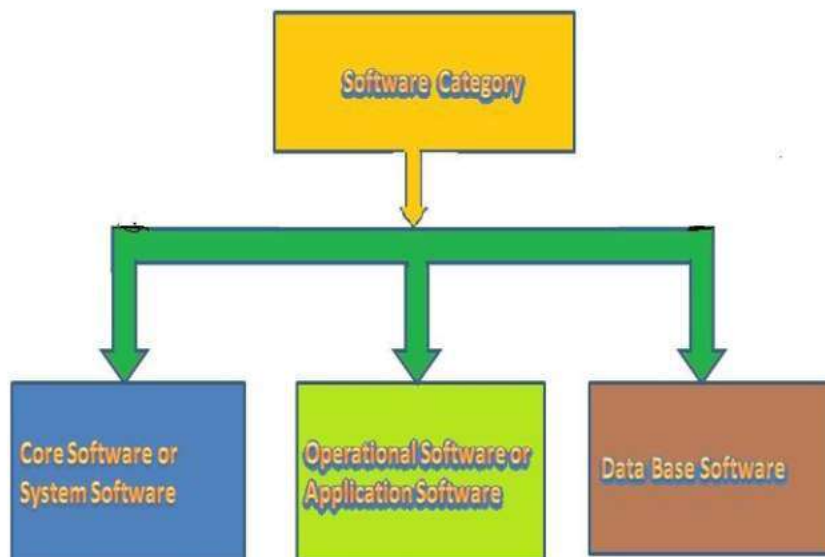
Figure13.1

Level	Type of failure	Failure description	Probability	Likelihood of failure (per flight hour)
A	Catastrophic failure	Aircraft loss and/or fatalities	Extremely improbable	Less than 10^{-9}
B	Hazardous/severe major failure	Flight crew cannot perform their tasks; serious or fatal injuries to some occupants	Extremely remote	Between 10^{-7} and 10^{-9}
C	Major failure	Workload impairs flight crew efficiency; occupant discomfort including injuries	Remote	Between 10^{-5} and 10^{-7}
D	Minor failure	Workload within flight crew capabilities; some inconvenience to occupants	Probable	Greater than 10^{-5}
E	No effect	No effect	Not applicable	

Table 13.1

5.14 ELECTROMAGNETIC ENVIRONMENT

Influence of the following phenomena on maintenance practices for electronic system: EMC-Electromagnetic Compatibility EMI- Electromagnetic Interference HIRF-High Intensity Radiated Field Lightning/lightning protection.

INTRODUCTION

The EME (electromagnetic environment) is a form of energy, which is the same type of energy (electrical) that is used by electrical/electronic equipment to process and transfer information. As such, this environment represents a fundamental threat to the proper operation of systems that depend on such equipment. Electrical/electronic systems, characterized as Level A, provide functions that can affect the safe operation of an aircraft and depend upon processed by electronic equipment.

Thus, the EME threat to such systems may translate to a threat to the airplane itself. The computers associated with modern aircraft guidance and control systems are susceptible to upset from lightning and sources that radiate RF at frequencies predominantly between 1 and 500 MHz and produce aircraft internal field strengths of 5 to 200 V/m or greater. Internal field strengths greater than 200 V/m are usually periodic pulses with pulse widths less than 10µs. Internal lightning-induced voltages and currents can range from approximately 50 V and 20 A to over 3000 V and 5000 A. Electrical/electronic system susceptibility to such an environment has been suspect as the cause of "Nuisance Disconnects", "Hardovers" and "upsets".

EME ENERGY SUSCEPTIBILITY

It is clear that the sources of electromagnetic (EM) threats to the electrical/electronic system, either digital or analog, are numerous. Although both respond to the same threats, there are factors that can make the threat response to a momentary transient (especially intense transients like those that can be produced by lightning) far more serious in digital processing systems than in analog systems. For example, the information bandwidth and, therefore, the upper noise response cutoff frequency in analog devices is limited to, at most, a few mega hertz. In digital systems it is often in excess of 100 MHz and continues to increase. This bandwidth difference, which is at least 10 times more severe in digital systems, allows substantially more energy and types of energy to be coupled into the digital system. Immunity of electronic components to damage is a consideration that occurs as part of the circuit design process. The circuit characteristic (immunity to damage) is influenced by a variety of factors:

1. Circuit impedances (resistance, inductance, capacitance), which may be distributed as well as lumped;

2. The impedances around system component interconnecting loops along with the characteristic (surge) impedance of wiring interfacing with circuit components;
3. Properties of the materials used in the construction of a component (e.g., thick-film/thin-film resistors);
4. Threat level (open circuit voltage/short circuit current), resulting in a corresponding stress on insulation, integrated circuit leads, PC board trace spacing, etc.; and
5. Semiconductor device nonlinearities (e.g., forward biased junctions, channel impedance, junction/gate breakdown).

Immunity to upset for analog processors is achieved through circuit design measures, and for digital processors it is achieved through architectural as well as circuit design measures.

SOFT FAULTS

Digital circuit upset, which has also been known by the digital computer or information processing community as a "soft fault," is a condition known to occur even in relatively benign operating environments. Soft faults occur despite the substantial design measures (timing margins, transmission line interconnects, ground and power planes, clock enablers of digital circuits) to achieve a relatively high degree of integrity in digital processor operation.

In a normal operating environment, the occurrence of soft faults within digital processing systems is relatively infrequent and random. Such occasional upset events should be treated as probabilistic in nature and can be the result of:

1. Coincidence of EME energy with clocked logic clock edges, etc.
2. Occasional violation of a device's operational margin (resulting margin from the design, processing, and manufacturing elements of the production cycle).

From this perspective, the projected effect of a substantial increase in the severity of the electromagnetic environment will be an increased probability of a soft fault occurrence. That is, in reality a soft fault may or may not occur at any particular point in time but, on the average, soft faults will occur more frequently with the new environmental level. Once developed, software is "burned into nonvolatile" memory (becomes "firmware"); the result will be a special purpose real-time digital electronic Technology data processing machine with the inherent potential for "soft faults." Because it is a hardware characteristic, this potential exists even when a substantial amount of attention is devoted to developing "error-free" operating system and application programs(s) (software) for the general purpose digital machine (computing platform, digital engine, etc.).

MEAN TIME BETWEEN UNSCHEDULED REMOVAL / MEAN TIME BETWEEN FAILURE

In general the disparity in mean time between unscheduled removal and the mean time between failure continues to be significant. The impact of this disparity on airline direct operating costs is illustrated in Figure-14.1.

To the extent that soft faults contribute to the MTBUR/MTBF disparity, any reduction in soft fault occurrence and propagation could translate into reduction of this disparity.

ELEMENTS OF EME

1. Lightning
2. HIRF
3. HIRF
4. EMC

The electrical and/or electronic systems that perform functions "critical" to flight must be identified by the applicant. This may be accomplished by conducting a functional hazard Assessment and, if necessary, preliminary system safety assessments.

The term "critical" means those functions whose failure would contribute to, or cause, a catastrophic failure condition (loss of aircraft). Table-14.1 provides the relationship between function failure effects and development assurance levels associated with those systems that implement functions that can affect safe aircraft operation.

The terms "Level A," etc. designate particular system development assurance levels. System development assurance levels refer to the rigor and discipline of processes used during system development (design, implementation, verification / certification, production, etc.). It was deemed necessary to focus on the development processes for systems based upon "highly integrated" or "complex" (whose safety cannot be shown solely by test and whose logic is difficult to comprehend without the aid of analytical tools) elements, i.e., primarily digital electronic elements. Development assurance activities are ingredients of the system development processes.

As has been noted, systems and appropriate associated components are assigned "development assurance levels" based on failure condition classification associated with aircraft-level functions implemented by systems and components.

Relative to safety, they are also categorized (from regulatory advisory material) by the effect of their failures, i.e., catastrophic, severe major/hazardous, major, etc. EMC has been included in Airworthiness Regulatory's regulations since the introduction of radio and electrical/electronic systems into aircraft.

1. Electrical equipment, controls, and wiring must be installed so that operation of any one unit, or system of units, will not adversely affect the simultaneous operation of any other electrical unit or system essential to aircraft safe operation.
2. Cables must be grouped, routed, and spaced so that damage to essential circuits will be minimized if there are faults in heavy current-carrying cables.
3. Radio and electronic equipment, controls, and wiring must be installed so that operation of any one component or system of components will not adversely affect the simultaneous operation of any other radio or electronic unit, or system of units, required by aircraft functions.

4. Relative to safety and electrical/electronic systems, the systems, installations, and equipment whose functioning is required for safe aircraft operation must be designed to ensure that they perform their intended functions under all foreseeable operating conditions.

Aircraft systems & associated components considered separately & in relation To other systems, must be designed so that:

1. The occurrence of any failure condition that would prevent the continued safe flight and landing of the airplane is extremely improbable.

2. The occurrence of any other failure condition that would reduce the capability of the airplane or the ability of the crew to cope with adverse operating conditions is improbable.
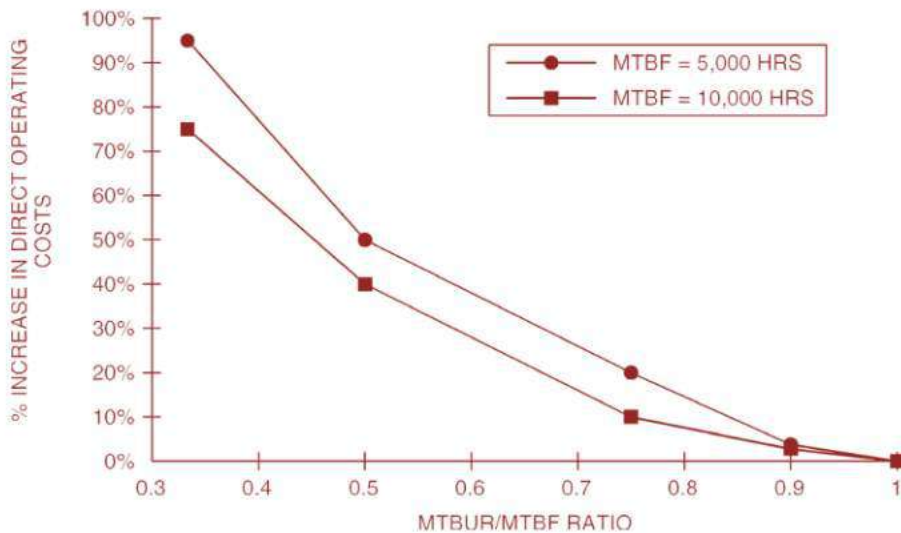
Figure 14.1 : MTBUR / MTBF Ratio Impact of Operating Costs

Failure Condition Classification	Development Assurance Level
Catastrophic	Level - A
Severe Major / Hazardous	Level - B
Major	Level - C
Minor	Level - D
No Effect	Level - E

Table14.1

ELECTROMAGNETIC INTERFERENCE

There are many sources of EMI throughout the aircraft. Those sources known to radiate EMI include:

a. Fluorescent lights.
b. Radio and radar transmitters.
c. Power lines.
d. AC powered window heat controllers.
e. Motors/generators.
f. Switching and light dimming circuits.

g. Microprocessors.

h. Pulsed high-frequency circuits.

i. Data bus cables (but not fibre optic cables)

j. Static discharge and lightning.

There are many systems on the aircraft that which may be susceptible to electromagnetic interference. These include:

a. Radio and radar receivers.

b. Microprocessors and other microelectronic systems.

c. Electronic instruments.

d. Control systems.

e. Audio and in-flight entertainment systems (IFE).

ELECTROMAGNETIC COMPATIBILITY (EMC)

Whether a system will have an adverse response to electromagnetic interference depends on the type and amount of emitted energy in conjunction with the susceptibility threshold of the receiving system. The threshold of susceptibility is the minimum interference signal level (conducted or radiated) that results in equipment performance that is indistinguishable from the normal operation. If the threshold is exceeded then the performance of the equipment will become degraded.

When the susceptibility threshold level is greater than the levels of radiated emissions, electromagnetic interference problems do not exist. Systems to which this applies have electromagnetic compatibility (EMC). In other words, the systems will operate as intended and any EMI generated is at such a level that it does not affect normal operation.

Planning for electromagnetic compatibility must be initiated in the design phase of a device or system. If this is not satisfactorily addressed, interference problems may arise. The three factors necessary to produce an EMI problem are:

a. Source(s) of interference (sometimes called noise).

b. A means of coupling (by conduction or radiation).

c. Susceptible components or circuits.

To reduce the effects of EMI, or electrical noise, at least one of these factors must be addressed. The following lists some techniques used for EMI reduction to tackle these three factors.

1. SUPPRESS THE INTERFERENCE AT SOURCE

a. Enclose the interference source(s) in a screened metal enclosure and then ensure that the enclosure is adequately grounded.

b. Use transient suppression on relays, switches and contactors.

c. Twist and/or shield bus wires and data bus connections.

d. Use screened (i.e. coaxial) cables for audio and radio- frequency signals.

e. Keep pulse rise times as slow and long as possible.

f. Check that enclosures, racks and other supporting structures are grounded effectively.

2. REDUCE NOISE COUPLING

a) Separate power leads from interconnecting signal wires.
b) Twist and/or shield noisy wires and data bus connections.
c) Use screened (i.e. coaxial) cables for audio and radio- frequency signals.
d) Keep ground leads as short as possible.
e) Pay close attention to potential ground loops.
f) Filter noisy output leads.
g) Physically relocate receivers and sensitive equipment away from interference sources.

2. INCREASE THE SUSCEPTIBILITY THRESHOLDS

a) Limit the bandwidth of circuits wherever possible.
b) Limit the gain and sensitivity of circuits wherever possible.
c) Ensure that enclosures are grounded and that internal screens are fitted.
d) Fit components that are inherently less susceptible to the effect of stray radiated fields.

HIRF

High-intensity/energy radiated Fields (HIRF/HERF) are generated by certain radio-frequency (RF) sources that are external to the aircraft. These Fields disrupt electronic components and systems within the aircraft via currents that are induced from these fields into the aircraft's wiring. The HIRF environment has become a signicant threat to aircraft using the electronic systems together with the communications, navigation and Flight guidance systems.

These systems are potentially very Susceptible to the HIRF environment. Accidents and incidents on aircraft with such systems have led to the need for a thorough understanding of, and increased protection from, high-intensity radiated Fields. HIRF has been cited as the cause of misleading roll and pitch information on electronic displays and the total loss of engine power due to interference with electronic control systems. The need for protection of modern electrical and electronic systems from HIRF is required because of the:

1. Dependence on these systems used for the continued safe flight and landing of the aircraft.
2. Increased use of composite materials (reducing the natural Faraday cage protection of metallic structures).
3. Increased complexity of digital systems (faster operating speeds, higher-density integrated circuits).
4. Expanded frequency usage of microwave energy.
5. Increased quantity and power of transmitters.
6. Proliferation of RF transmitters.

HIRF ENVIRONMENT

The HIRF environment is created by the transmission of high- power radio-frequency (RF) energy free space. These transmissions can be from military systems, television, radio, radars and satellites

communicating with ground-based equipment, ships or other aircraft. When an aircraft operates in a HIRF environment, this can have an adverse effect on the aircraft systems and equipment that could result in system failure, malfunction, or misleading information.

The process where by electromagnetic energy from an RF source is induced in a system by radiation is termed coupling. It is entirely possible that HIRF will affect individual components through to system level via individual wires (or wire bundles) that connect the items of equipment. In the event of the HIRF environment having an adverse effect on systems, it is essential that the aircraft has the capability for continued controlled flight and landing to a suitable location, albeit under emergency conditions.

PROPERTIES OF HIRF

The analysis of HIRF is centered on the frequency of transmission and field strength.

The practical considerations of RF transmissions are from approximately 10 kilohertz (10 kHz) through to 100 gigahertz (100 GHz). Field strength is defined as the magnitude of the electromagnetic energy propagating in free space expressed in volts per meter (V/m). Aircraft systems need to be tested and/or analysed across a range of frequencies and field strengths to determine their susceptibility characteristics. Certain systems (or individual items of equipment) are immune to HIRF and have the ability to continue to perform their intended function. This could occur as an inherent or system design feature of the equipment, e.g. if is located behind a material (reflection plane) that reflects RF signals.

Alternatively, a decrease in electromagnetic field strength in transmission from one point to another can occur by attenuation, expressed in decibels (dB). Attenuation is the scalar ratio of the RF energy input magnitude and output magnitude. (Further details of attenuation are given in the appendices). In the HIRF environment, the ratio of current induced in a wire bundle form the external HIRF field strength (as a function of frequency) is termed the transfer function An item of equipment or system that is susceptible to the HIRF environment means that it is unable to perform its intended function; this will be defined by a susceptibility level, where the effects of interference from HIRF become apparent.

LIGHTNING

Lightning together with precipitation is associated with electrical activity within cumulonimbus clouds, see figure-14.2.

Lightning results from the buildup of huge amounts of static charge in the atmosphere.

Precipitation may defined as the result of water vapour condensing in the atmosphere that subsequently falls to the earth's surface. Electrical activity can originate at the top of thunder clouds or the outside edges of the precipitation area. If an aircraft is subjected to a lightning strike, or discharge, the structure and bonding are designed to dissipate this energy, see Figure 14.3.

Within the structure to redistribute themselves so as to cancel the field's effects inside the fuselage. This effect is used very effectively in aircraft to protect electronic equipment from lightning strikes and other electrostatic discharges. Lightning normally enters the aircraft at an extremity, e.g. the nose cone or wing tip; currents flow through the conductive structure, and then exits the aircraft at

another extremity. This can cause short-term interference with systems, but there should be no permanent damage.

Some currents could enter the structure due to the high voltages; the energy will normally be conducted through bonding leads and back into the fuselage skin. The aircraft is categorized into specific areas when planning system and equipment locations, see Fig.-3.

1. Zone one is where lightning can be expected to enter and exit the aircraft
2. Zones two and three provide the conductive paths through the aircraft.

Figure-14.2, Electrical Storm
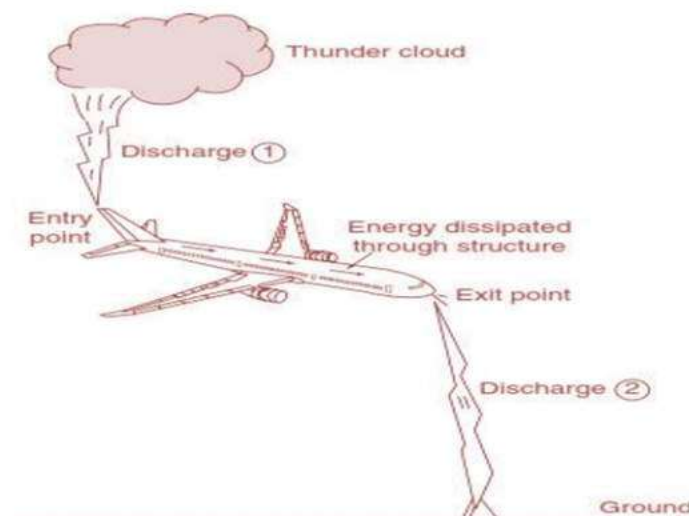
Figure 14.3: Lightning Strike; Dissipation of Energy through the Aircraft (Electrical & Magnetic Fields)

HIRFL EFFECTS

The following factors, have led to this concern about lightning and HIRF effects:

1. Reduction of the operating power level of electronic devices that may be used in electrical and electronic systems, which may cause circuits to be more reactive to induced lightning and RF voltages and currents leading to malfunction or failure.
2. Increased percentage of composite materials in aircraft construction. Because of their decreased conductivity, composite materials may result in less inherent shielding by the aircraft structure.

3. . Since current flowing in the lightning channel will be forced (during lightning attachment) into and through the aircraft structure without attenuation, decreased conductivity for aircraft structure materials can be particularly troubling for lightning.
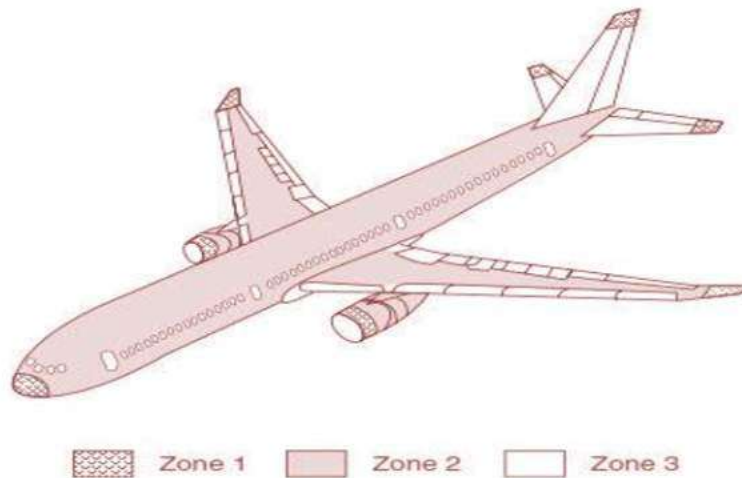
Figure 14.4 Lightning zone

LIGHTNING PROTECTION

RADOME PROTECTION

The metal structure dissipates electric currents generated from the external electromagnetic fields, thereby reducing or even eliminating electromagnetic interference. More aircraft are now being built using (non-conducting) composite materials, ranging from individual items of structure through to the complete exterior. In this case, the Faraday cage effect has to be designed into the composite structure as a mess of conducting material. Additional design effort, testing and on-going maintenance are required as a consequence. One particular part of the aircraft often affected by lighting is the nose cone; this is made from a composite material and therefore has no inherent conductive paths. Lightning strips can be fitted to protect this area, see Figure 14.5.
Even when the lightning discharge is dissipated safely through the aircraft, structural damage can occur at the exit points of the discharge. Furthermore, the high circulating currents can causes EMI as previously discussed. Lightning discharges via the atmosphere from one cloud to another, or directly to the earth's surface.

The atmosphere has a very high dielectric breakdown (depending on moisture content), typically three million volts per meter. The voltage generated by lightning depends on the length travelled by the lightning discharge; this will be approximately one gigavolt for a 300 m (1000ft) lightning bolt. With a typical current of 100 kA, this gives rise to a power dissipation of 100 terawatts(1000 X 1 012 watts). The high energy radiated by a lightning discharge carries sufficient electromagnetic field strength to couple into the aircraft's wiring. This causes high currents of relatively short duration to be injected into electronic equipment. Adequate protection must be designed into the equipment to prevent disruption of signal processing and/or damage to components.
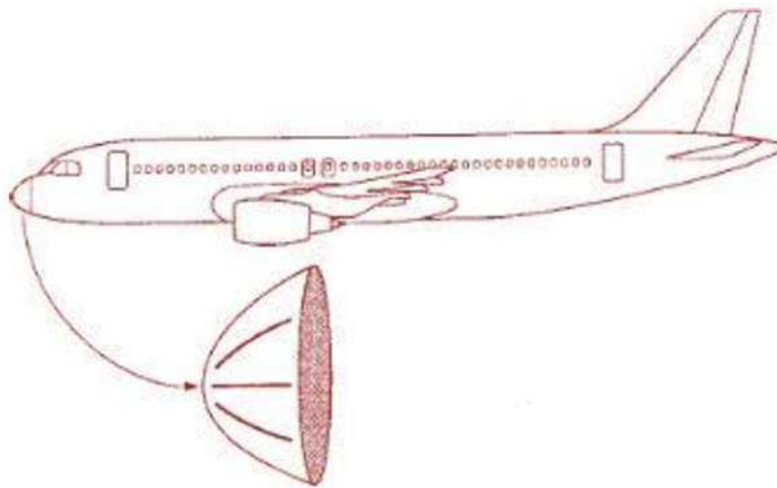
Figure 14.5 Radome Protection

PROPAGATION OF ELECTROMAGNETIC ENVIRONMENT

Lightning and HIRF are threats to the overall aircraft. Since they are external EME elements, of the two, lightning produces the most intense environment, particularly by direct attachment. Both lightning and HIRF interactions produce internal fields. Lightning can also produce substantial voltage drops across the aircraft structure. Such structural voltages provide another mechanism (in addition to internal fields) for energy to propagate into electrical/electronic systems. Also, the poorer the conductivity of structural materials, the greater the possibility that there are voltage differences across the structure, Significant lightning diffusion magnetic fields, Propagation of external environment energy.
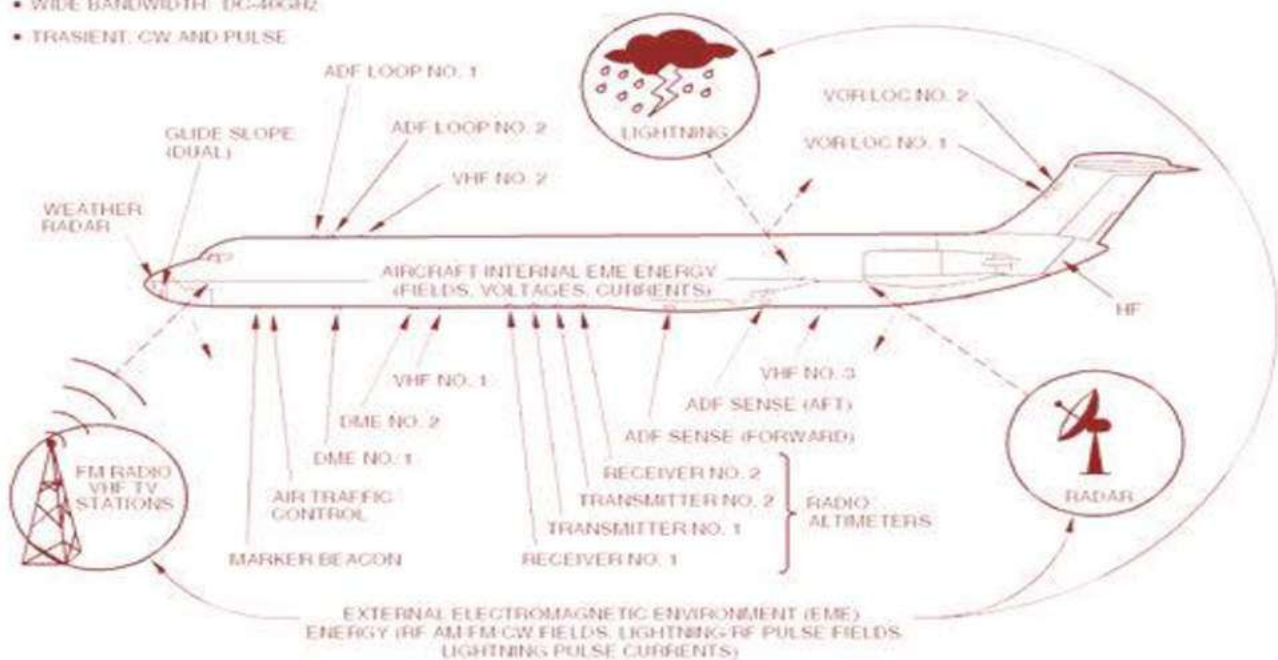
Figure 14.6: EM Environment on Aircraft Structure

Aircraft/installation features of interest. In general, the propagation of external EME energy into the aircraft interior and electrical/electronic systems is a result of complex interactions of the EME with the aircraft exterior structures, interior structures, and system installations (see Figure 14.7 to 14.11.
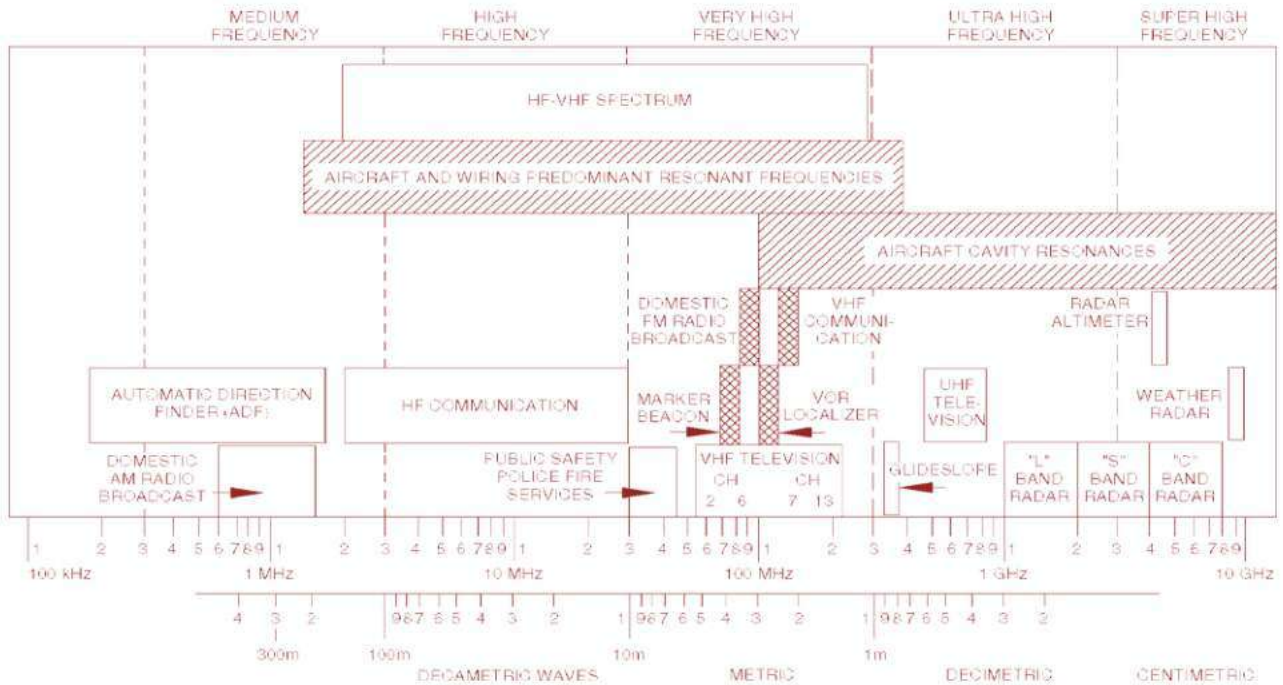
Figure 14.7

Paths of electromagnetic wave entry from the exterior to the interior equipment regions are sometimes referred to as points of entry. Examples of points of entry may be seams, cable entries, windows, etc. As noted, points of entry are driven by the local environment, not the incident environment. The internal field levels are dependent on both the details of the point of entry and the internal cavity.
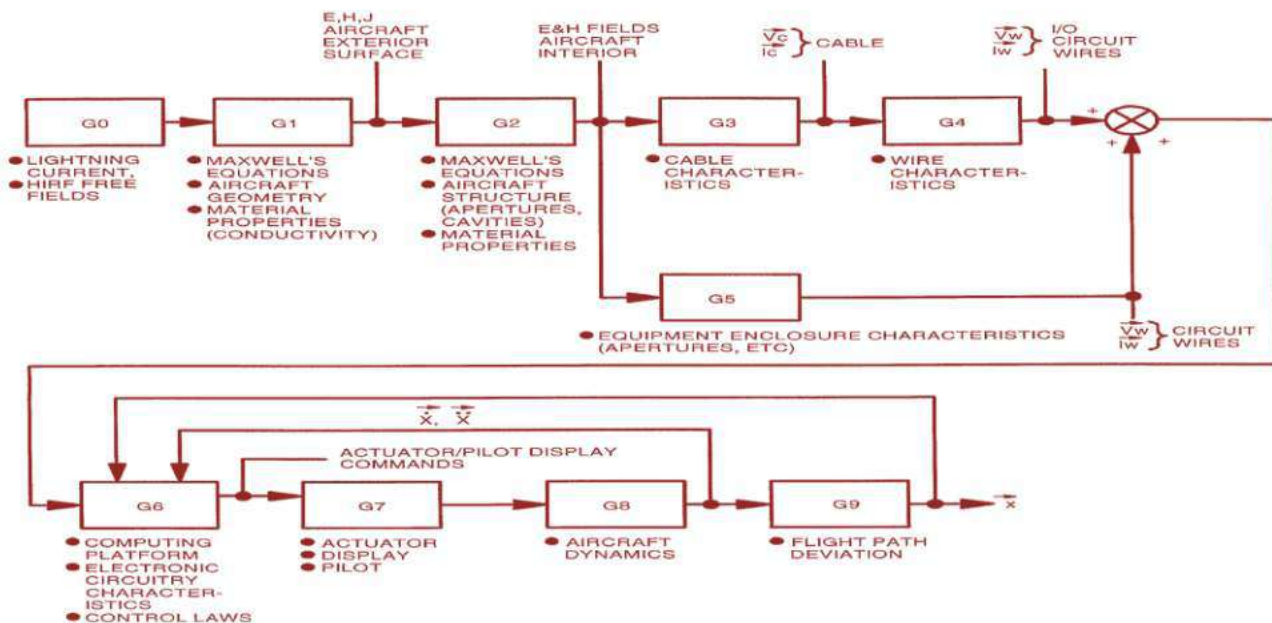
Figure 14.8: EME Propagation Process Transfer Function Perspective
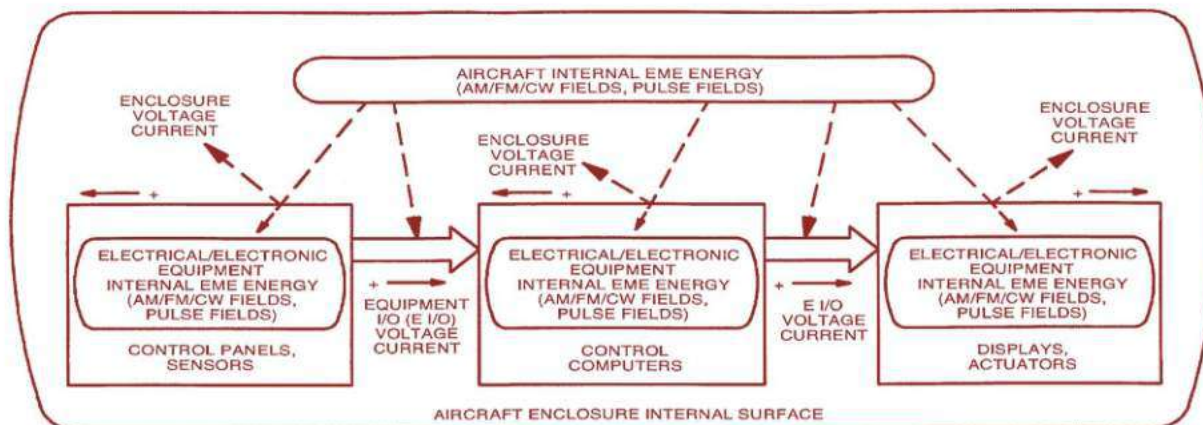
- External energy penetrates to interior via apertures, composites, seams, joints, and antennas
- Voltages and currents induced on flight control system components and cables
  - RF energy below 1 megahertz - induced coupling at these frequencies is inefficient and thus will probably be of lesser concern
  - RF energy between 1 and 300 megahertz is of major concern as aircraft wiring, when their lengths are on the order of a wavelength divided by two ($\lambda/2$) or longer at these frequencies, acts as a highly efficient antenna
  - RF energy coupling to aircraft wiring drops off at frequencies above 300 megahertz (at these higher frequencies, the EM energy tends to couple through box apertures rather than through aircraft wiring)

Figure 14.9: Aircraft Internal EME Energy Electrical / Electronic System

Resulting internal fields can vary over a wide range of intensity, wave shape, and wave impedance. (Below 10 MHz within a metal aircraft, the magnetic fields due to lightning predominate because of the electric field shielding properties of metal skins. For HIRF "high-frequency" bands in some internal regions, internal field levels may exceed the incident field levels.)
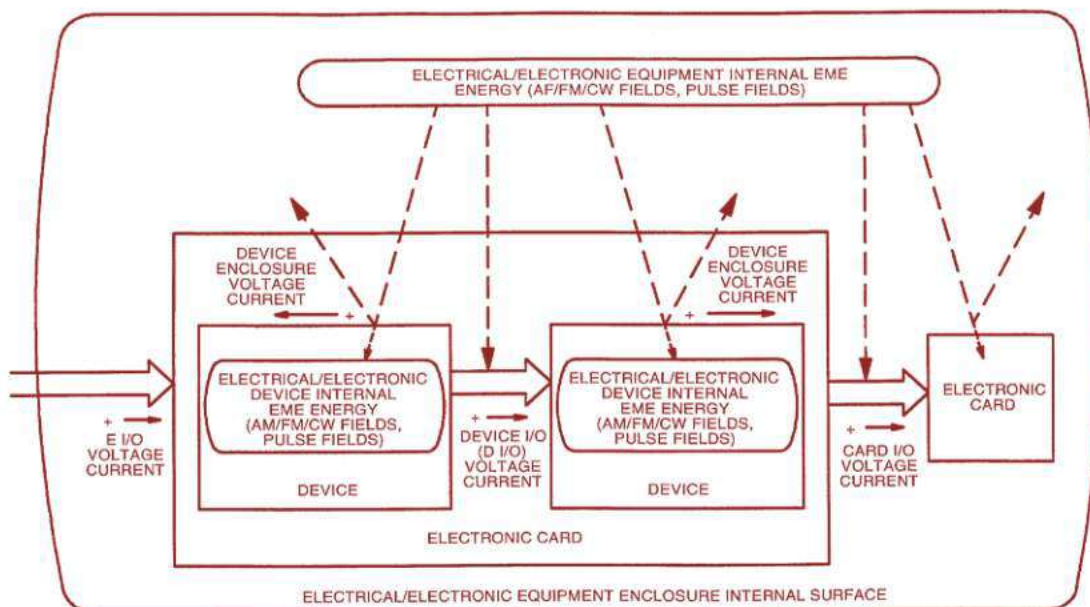
- Voltage, fields, currents and charge on system components penetrate into equipment enclosure interiors via holes, seams, and airplane wiring (cables)
- Energy (voltage and current) picked up by wires and printed conductors on cards and carried to electronic devices

Figure 14.10: Electrical / Electronic Equipment Internal EME Interaction Electrical / Electronic Circuitry
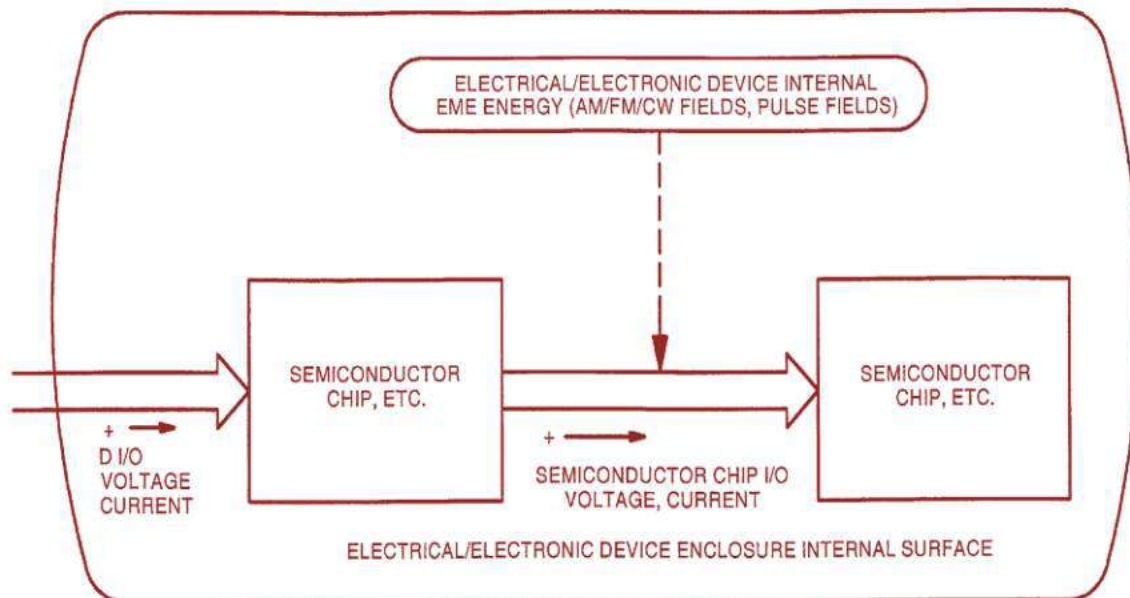
- Card and device conductors carry energy to the semiconductor chips, etc.
- Possible effects
  - Damage
  - Upset

Figure 14.11: Electrical / Electronic Device Internal EME Interaction Electrical / Electronic Circuitry

MAINTENANCE FOR HIRF / L PROTECTION

The maintenance engineer has a number of essential tasks to ensure that HIRF/L protection features and devices are serviceable for continued airworthiness of the aircraft. These tasks include, but are not limited to:

1. Bonding resistance measurements.
2. Wire/cable resistance or impedance measurements.
3. Inspection and disassembly of connectors to detect corrosion or termination failure.

BONDING AND GROUNDING

Bonding and grounding connections are made in an aircraft in order to accomplish the following:

1. Dissipate energy from a high-intensity radiated fields (HIRF) and lightning strikes.
2. Dissipate static electricity.
3. Limit the potential difference between equipment.
4. Provide a low resistance path for earth return systems.

Figure 14.12: Equipment's bonding

1. EQUIPMENT BONDING

Low impedance paths to the aircraft structure are generally required for electronic equipment to provide radio-frequency return circuits and to facilitate reduction in EMI.

2. METALLIC SURFACE BONDING

All conducting objects located on the exterior of the airframe should be electrically connected to the airframe through mechanical joints, conductive hinges, or bond straps, which are capable of conducting static charges and currents induced by lightning strikes.

3. STATIC BONDS

All isolated conducting paths inside and outside the aircraft with an area greater than 3 in.^{2} and a linear dimension over 3 inches that are subjected to electrostatic charging should have a mechanically secure electrical connection to the aircraft structure of adequate conductivity to dissipate possible static charges.

Figure 14.13

5.15 TYPICAL ELECTRONIC/DIGITAL AIRCRAFT SYSTEMS

Major avionic systems fitted to a modern passenger aircraft which includes:
- Aircraft Communication Addressing and Reporting System (ACARS)
- Electronic Centralized Aircraft Monitoring (ECAM)
- Electronic Flight Instrument System (EFIS)
- Engine Indication and Crew Alerting System (EICAS)
- Fly by Wire (FBW)
- Flight Management System (FMS)
- Global Positioning System (GPS)
- Inertial Reference System (IRS)
- Inertial Navigation System (INS)
- Traffic Alert Collision Avoidance System (TCAS)

To detect faults on these systems:
- Built-in Test Equipment (BITE).
- Automatic Test Equipment (ATE)

AIRCRAFT COMMUNICATION ADDRESSING AND REPORTING SYSTEM (ACARS)

ACARS is a digital data link system transmitted in the VHF range (129 MHz to 137 MHz). ACARS provides a means by which aircraft operators can exchange data with an aircraft without human intervention. This makes it possible for an airline to communicate with the aircraft in their fleet in much the same way as it is possible to exchange data using a land-based digital network. ACARS uses an aircraft's unique identifier and the system has some features that are similar to those currently used for electronic mail.

The ACARS system was originally specified in the ARINC 597 standard but has been revised as ARINC 724B. A significant feature of ACARS is the ability to provide real-time data on the ground relating to aircraft performance (see Fig. 15.1). This has made it possible to identify and plan aircraft maintenance activities. ACARS communications are automatically directed through a series of ground based ARINC (Aeronautical Radio Inc.) computers to the relevant aircraft operator. The system helps to reduce the need for mundane HF and VHF voice messages and provides a system which can be logged and tracked. Typical ACARS messages cater for the transfer of routine information such as:

- Passenger loads
- Departure reports
- Arrival reports

- Fuel data
- Engine performance data.

```
ACARS mode: E Aircraft reg: N27015
Message label: H1 Block id: 3
Msg no: C36C
Flight id: CO0004
Message content:-
#CFBBY ATTITUDE INDICATOR
MSG 2820121 A 0051 06SEP06 CL H PL
DB FUEL QUANTITY PROCESSOR UNIT
MSG 3180141 A 0024 06SEP06 TA I 23
PL
DB DISPLAYS-2 IN LEFT AIMS
MSG 2394201 A 0005 06SEP06 ES H PL
MSG 2717018
```

Figure 15.1 Example of a downlink ACARS message sent from a Boeing 777aircraft

```
ACARS mode: 2
Aircraft reg: G-DBCC
Message label: 5U
Block id: 4
Msg no: M55A
Flight id: BD01NZ
Message content:-
01 WXRQ 01NZ/05 EGLL/EBBR .G-DBCC
/TYP 4/STA EBBR/STA EBOS/STA EBCI
```

Figure 15.2 Example of an ACARS message

Frequency	ACARS Service
129.125 MHz	USA and Canada (Additional)
130.025 MHz	USA and Canada (Secondary)
130.450 MHz	USA and Canada (Additional)
131.125 MHz	USA (Additional)
131.475 MHz	Japan (Primary)
131.525 MHz	Europe (Secondary)
131.550 MHz	USA, Canada, Australia (Primary)
131.725 MHz	Europe (Primary)
136.900 MHz	Europe (Additional)

Table 15.1 : ACARS Channels

This information can be requested by the company and retrieved from the aircraft at periodic intervals or on demand. Prior to ACARS this type of information would have been transferred via VHF voice communication. ACARS uses a variety of hardware and software components including those which are installed on the ground and those which are present in the aircraft. The aircraft ACARS components include a Management Unit which deals with the reception and transmission of messages via the VHF radio transceiver, and the Control Unit which provides the crew interface and consists of a display screen and printer. The ACARS Ground Network comprises the ARINC ACARS remote transmitting/receiving stations and a network of computers and switching systems. The ACARS Command, Control and Management Subsystem consists of the ground based airline operations and associated functions including operations control, maintenance and crew scheduling. There are two types of ACARS messages; downlink messages that originate from the aircraft and uplink messages that originate from ground stations. The data rate is low and messages comprise plain alphanumeric characters. Frequencies used for the transmission and reception of ACARS messages are in the band extending from 129 MHz to 137 MHz (VHF) as shown in Table 15.1 above. Note that different channels are used in different parts of the world. A typical ACARS message (see Fig. 15.2) consists of :

- Mode Identifier (e.g. 2)
- Aircraft Identifier (e.g. G-DBCC)
- Message Label (e.g. 5U)
- Block Identifier (e.g. 4)
- Message Number (e.g. M55A)
- Flight Number (e.g. BD01NZ)
- Message Content

ELECTRONIC FLIGHT INSTRUMENT SYSTEM (EFIS)

As mentioned in Chapter 1, most modern passenger aircraft use Electronic Flight Instrument System (EFIS) displays in that has become known as the 'glass cockpit' (see Figure 15.3). EFIS provides large, clear, high-resolution displays which are easy to view under wide variations of ambient light intensity. Displays can be independently selected and configured as required by the captain and first officer and the ability to display information from various data sources in a single display makes it possible for the crew to rapidly assimilate the information that they need. The EFIS uses input data from several sources including:

- VOR / ILS / MLS
- TACAN (See Later)
- Pitch, roll, heading rate and acceleration data from an Attitude Heading System Reference (AHRS) or conventional vertical gyro
- Compass System
- Radar Altimeter
- Air Data System

- Distance Measuring Equipment (DME)
- Area Navigation System (RNAV)
- Vertical Navigation System (VNAV)
- Weather Radar System (WXR)
- Automatic Direction Finder (ADF

Figure 15.3: A320 PFD and ND Brightness and Transfer Controls

Figure 15.4: Boeing 757 EICAS

ENGINE INDICATING AND CREW ALERTING SYSTEM (EICAS)

The Engine Indication and Crew Alerting System (EICAS) are designed to provide all engine instrumentation and crew annunciations in an integrated format. The equivalent system on Airbus aircraft is the Electronic Centralized Aircraft Monitoring (ECAM) system. The information supplied by EICAS/ECAM includes display of engine torque, inter-stage turbine temperature, high and low pressure gas generator RPM, fuel flow, oil temperature and pressure. As part of the EICAS, graphical depiction of aircraft systems can be displayed. Such systems as electrical, hydraulic, de-icing, and environmental and control surface position can be represented. All aircraft messages relating to these systems are also displayed on the EICAS. Improves reliability through elimination of traditional engine gauges and simplifies the flight deck through fewer standalone indicators. EICAS also reduces crew workload by employing a graphical presentation that can be rapidly assimilated. EICAS can also help to reduce operating costs by providing maintenance data. A

typical EICAS comprises two large higher solutions, color displays together with associated control panels, two or three EICAS data concentrator units and a lamp driver unit. The primary EICAS display presents primary engine indication instruments and relevant crew alerts. It has a fixed format providing engine data including:

- RPM and Temperature
- Fuel Flow and Quantity Engine Vibration
- Gear and Flap Details (Where Appropriate)
- Caution Alerting System (CAS) Messages (color coded to indicate importance)

The secondary EICAS display indicates a wide variety of options to the crew and serves as a backup to the primary display. They are selectable in pages using the EICAS control panel and include the display of information relating to:

- Landing Gear Position
- Flaps / Trim
- Auxiliary Power Unit
- Cabin Pressurization / Anti-ice
- Fuel / Hydraulics
- Flight Control Positions
- Doors / Pressurization / Environmental
- AC and DC Electrical Data

The EICAS displays receive data bus inputs from the EICAS Data Conversion Unit (DCU). The EICAS displays provide data bus outputs to the Integrated Avionics Processing System (IAPS) Data Concentrator Units (DCU). Note that the pilot or co-pilot can select either display. Selecting one display blanks the second display and allows data pages to be selected. The EICAS control (ECU) panel is used to select pages. The information on the data buses is routed to both EICAS displays and both multifunction displays. The DCU receives data in various formats from a variety of sensors, including the high and low speed unit. The Lamp Driver Unit (LDU) is a dual channel unit capable of driving up to 120 indicator lamps. Channels 1 and 2 receive digital buses from all the DCU. The buses convey lamp activation words from the DCU. Channels 1 and 2 are identical and the outputs from each side are tied together (wired-OR logic). If one channel lamp sink fails, the other channel lamp sink will provide the function. The LDU monitors the lamp sinks to verify correct function and outputs the lamp sink states on a digital bus to the DCU. The Electronic Routing Units (ERU) are junction boxes for the data concentrator units. The ERU splits each input signal to three output pins. The pilot ERU routes left-side airplane data and the co-pilot ERU routes right-side airplane data. EICAS simplifies flight deck clutter by integrating the many electro-mechanical instruments that previously monitored engine and aircraft systems. Safety is increased whilst the pilot workload is simplified. EICAS continuously monitors the aircraft for out-of-tolerance or abnormal conditions and notifies the crew when an event occurs. ARINC 429 bus, from analogue and discrete inputs from the engines and other aircraft systems. These are concentrated and processed for transmission on system buses (ARINC or otherwise). Outputs include crew alerting logic, engine data to the displays, maintenance, diagnostic and aircraft data to the IAPS DCU,

indicator lamp data to the LDU, aircraft system data to the Flight Data Recorder (FDR) and data link management.
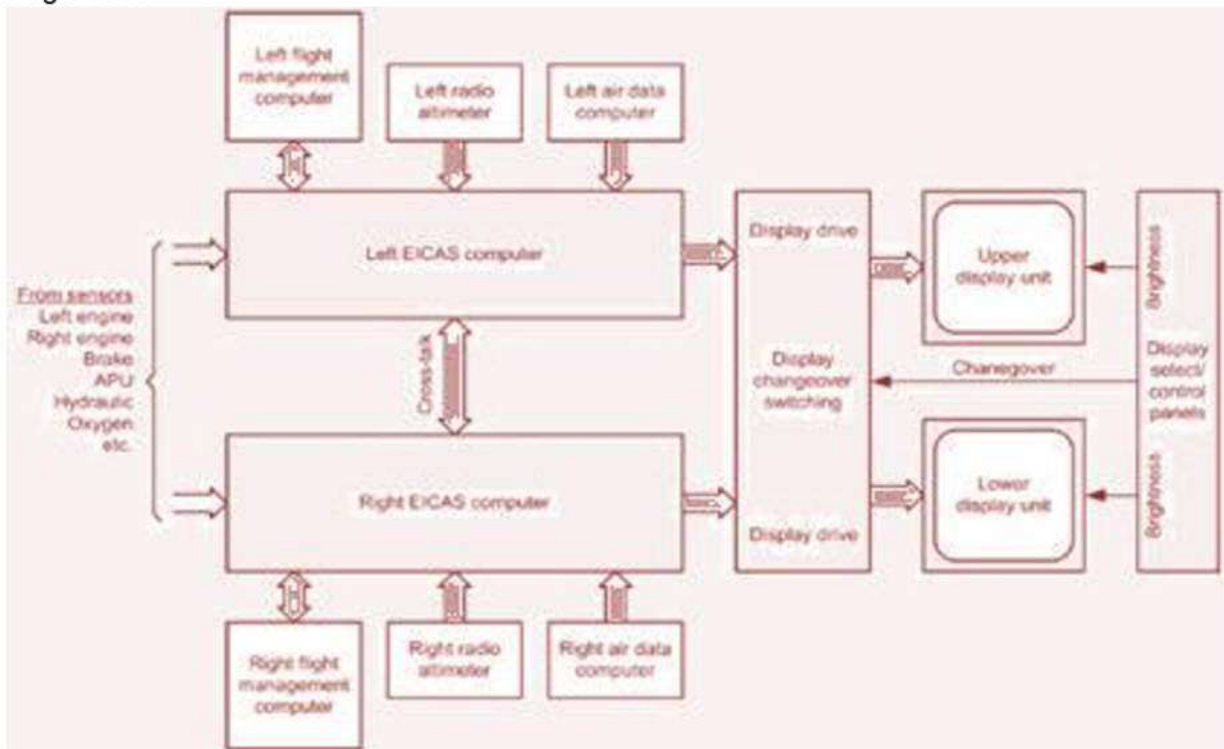
Figure 15.5: EICAS Simplified Block Schematic

FLY BY WIRE SYSTEM

The first electrical flight control system for a civil aircraft was designed by Aerospatiale and installed on the Concorde. This is an analog, full-authority system for all control surfaces. The first generation of electrical flight control systems with digital technology appeared on several civil aircraft at the start of the 1980s with the Airbus A310 program. These systems control the slats, flaps, and spoilers. The Airbus A320 (certified in early 1988) is the first example of a second generation of civil electrical flight control aircraft, rapidly followed by the A340 aircraft (certified at the end of 1992). The distinctive feature of these aircraft is that all control surfaces are electrically controlled and that the system is designed to be available under all circumstances. "Fly-by-wire" technology translates the pilot's actions into electronic signals, which computers use to manipulate flight controls. The computers constantly monitor pilot input and prevent the aircraft from exceeding its flight envelope, thereby increasing safety. And because fly-by-wire replaces heavy, complex mechanical linkages with lighter electrical wires, it is more efficient.

NEED OF FLY BY WIRE SYSTEM

CONVENTIONAL PRIMARY FLIGHT CONTROLS SYSTEMS

This system employ hydraulic actuators and control valves controlled by cables that are driven by the pilot controls. These cables run the length of the airframe from the cockpit area to the surfaces to

be controlled. This type of system, while providing full airplane control over the entire flight regime, does have some distinct drawbacks. [See figure 15.6 (a) and (b)].
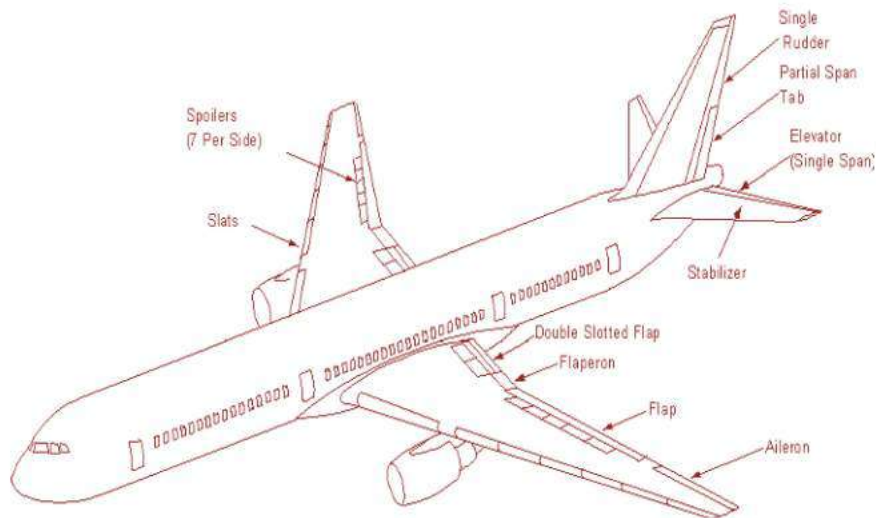
Figure 15.6 (a): Aircraft Flight Control Surfaces
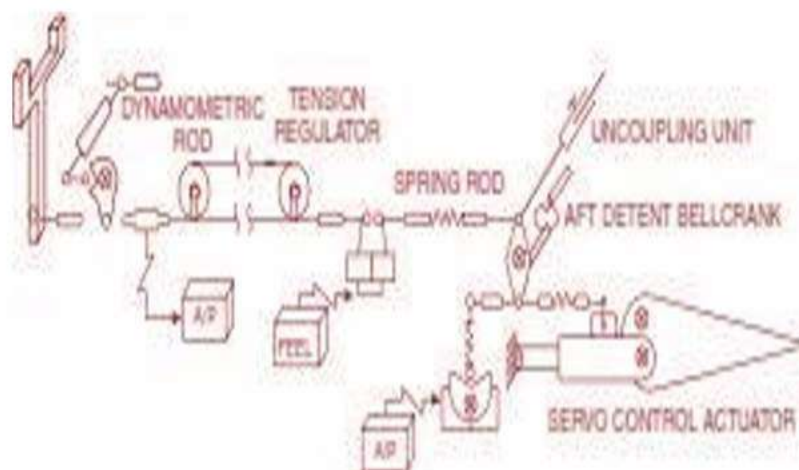
Figure 15.6 (b): Aircraft Mechanical Flight Controls

The cable-controlled system comes with a weight penalty due to the long cable runs, pulleys, brackets, and supports needed. The system requires periodic maintenance, such as lubrication and adjustments due to cable stretch over time. In addition, systems such as the yaw damper that provide enhanced control of the flight control surfaces require dedicated actuation, wiring, and electronic controllers. This adds to the overall system weight and increases the number of components in the system.

FBW FLIGHT CONTROL SYSTEM

In this system cable control of the primary flight control surfaces has been removed. Rather, the actuators are controlled electrically. At the heart of the FBW system are electronic computers.

These computers convert electrical signals sent from position transducers attached to the pilot controls into commands that are transmitted to the actuators. Because of these changes to the system, the following design features have been made possible:

- Full-time surface control utilizing advanced control laws. The aerodynamic surfaces of an aircraft have been sized to afford the required airplane response during critical flight conditions.
- The reaction time of the control laws is much faster than that of an alert pilot. Therefore, the size of the flight control surfaces could be made smaller than those required for a conventionally controlled airplane. This results in an overall reduction in the weight of the system.
- Retention of the desirable flight control characteristics of a conventionally controlled system and the removal of the undesirable characteristics.
- Integration of functions such as the yaw damper into the basic surface control. This allows the separate components normally used for these functions to be removed.
- Improved system reliability and maintainability.

NOTE: SPOILERS 4 AND 11 ARE COMMANDED VIA CABLES FROM THE CONTROL WHEEL AND VIA THE ACES FROM THE SPEED BRAKE LEVER. THE STABILIZER IS COMMANDED VIA THE CABLES THROUGH THE AISLE STAND LEVERS ONLY AND OTHERWISE IS COMMANDED THROUGH THE ACES.
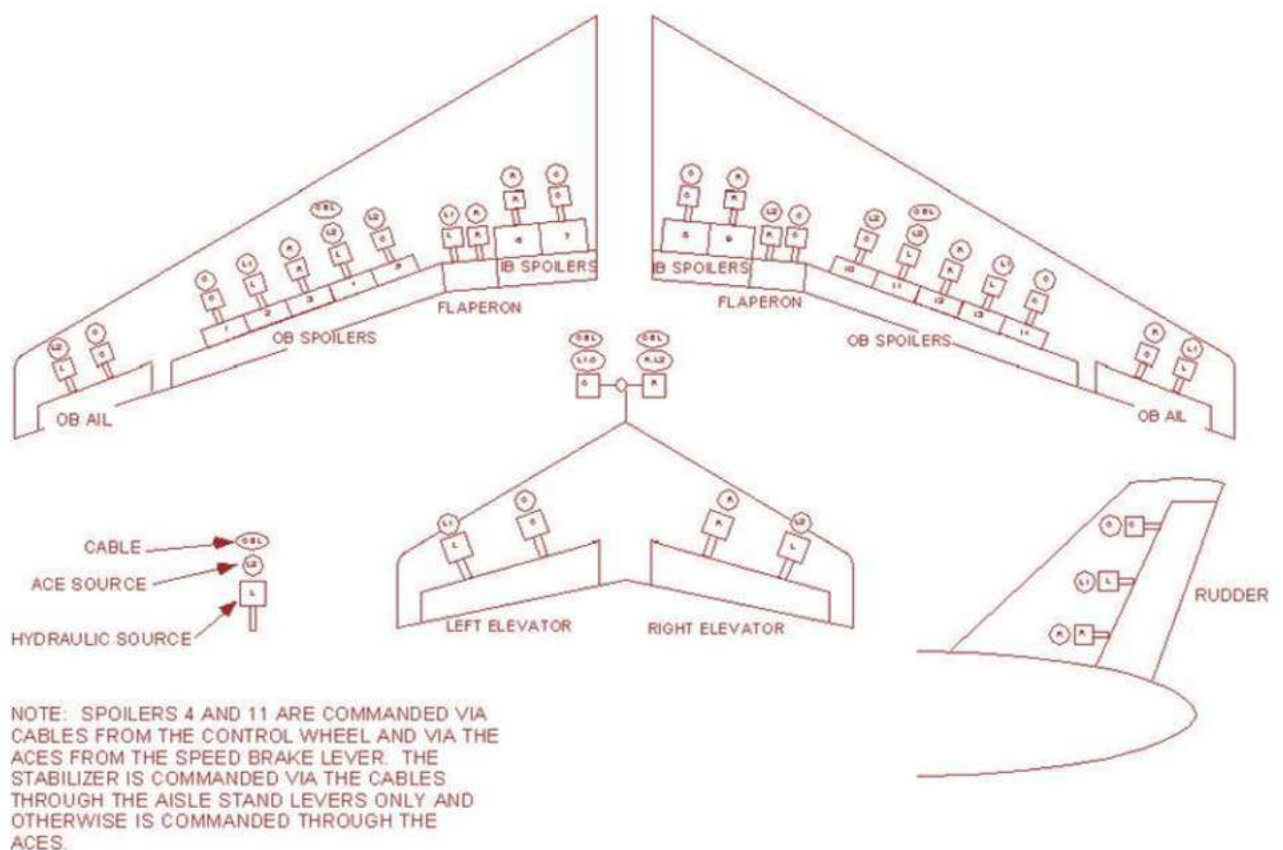
Figure-15.7   Schematic Representation of Mechanical Controls

Apart from above said features this Primary Flight Control System also include features such as:
- Bank Angle Protection
- Turn Compensation
- Stall and Over speed Protection
- Pitch Control and Stability Augmentation
- Thrust Asymmetry Compensation
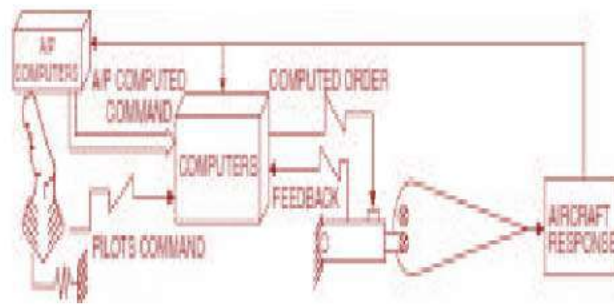
Figure 15.8: Electrical Flight Controls (FBW)

ADVANTAGE FBW FLIGHT CONTROL SYSTEM

A FBW flight control system has several advantages over a mechanical system. These include:
1. Overall reduction in airframe weight.
2. Integration of several federated systems into a single system.
3. Superior airplane handling characteristics.
4. Ease of maintenance.
5. Ease of manufacture.

Greater flexibility for including new functionality or changes after initial design and production.

SYSTEM'S ELECTRONICS

There are two types of electronic computers used in the Primary Flight Control System:
1. The Actuator Control Electronics (ACE)
2. The Primary Flight Computer (PFC), which utilizes digital technology.

THE ACTUATOR CONTROL ELECTRONICS

This is primarily an analog device. The function of the ACE is to interface with the pilot control transducers and to control the Primary Flight Control System actuation with analog servo loops. All the Primary Flight Control System onboard maintenance capabilities. Four identical ACEs are used in the system, referred to as L1, L2, C, and R. These designations correspond roughly to the left, center, and right hydraulic systems on the airplane. The ACEs convert the transducer position into a digital value and then transmit that value over the ARINC 629 data busses for use by the PFCs.

THE PRIMARY FLIGHT COMPUTER

Which utilizes digital technology. The role of the PFC is the calculation of control laws by converting the pilot control position into actuation commands, which are then transmitted to the ACE. The PFC also contains ancillary functions, such as system monitoring, crew annunciation. There are three PFCs in the system, referred to as L, C, and R. The PFCs use these pilot control and surface positions to calculate the required surface commands. At this time, the command of the automatic functions, such as the yaw damper rudder commands, are summed with the flight deck

control commands, and are then transmitted back to the ACEs via the same ARINC 629 data busses. The ACEs then convert these commands into analog commands for each individual actuator.

COMMUNICATION BETWEEN ACE AND PFC

The communication between the ACE & PFC and with all other system of aircraft is via triplex, bi-directional ARINC 629 Flight Controls data busses, referred to as L, C, and R(Left, Center and Right). The connection from these electronic units to each of the data busses is via a stub cable and an ARINC 629 coupler.

COMMUNICATION WITH THE OTHER AIRPLANE SYSTEMS

The Airbus aircraft fly-by-wire systems use the information of three air data and inertial reference units (ADIRUs), as well as specific accelerometers and rate gyros and in Boeing, the Primary Flight Control System transmits and receives data from other airplane systems by two different pathways.

- The Air Data and Inertial Reference Unit (ADIRU), Standby Attitude and Air Data Reference Unit (SAARU), and the Autopilot Flight Director Computers (AFDC) transmit and receive data on the ARINC 629 flight controls data busses, which is a direct interface to the Primary Flight Computers.
- The Flap Slat Electronics Unit (FSEU), Proximity Switch Electronics Unit (PSEU), and Engine Data Interface Unit (EDIU) transmit and receive their data on the ARINC 629 systems data busses.

The PFCs receive data from these systems through the Airplane Information Management System (AIMS) Data Conversion Gateway (DCG) function. The DCG supplies data from the systems data busses onto the flight controls data busses.
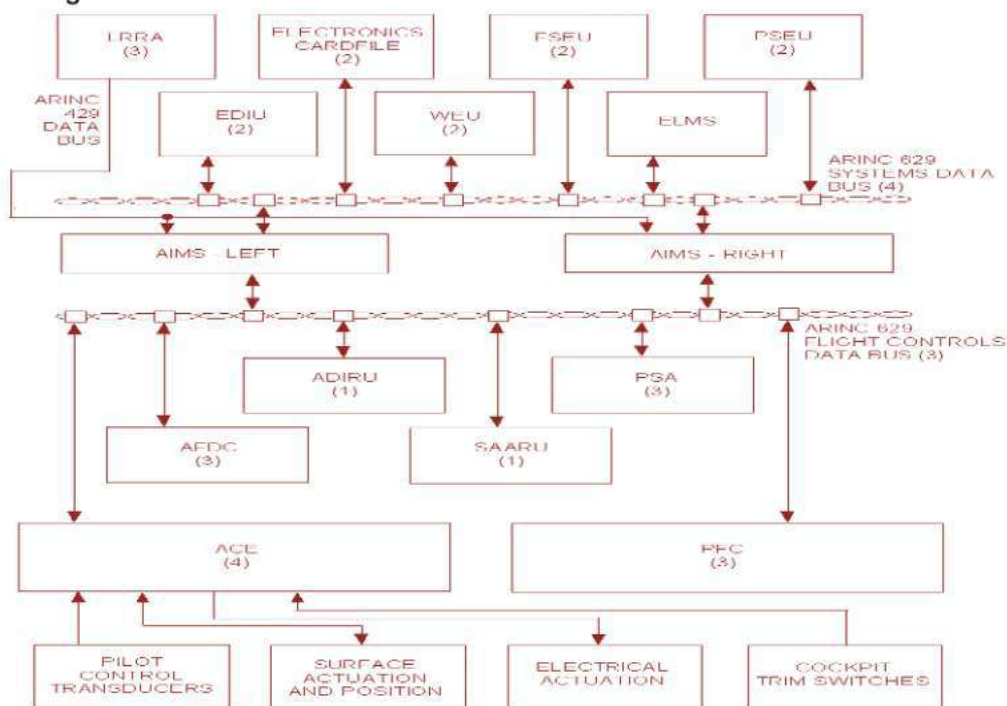

Figure 15.9: Block diagram of the electronic components of the Primary Flight Control System, as well as the interfaces to other airplane systems

MODE OF OPERATION OF FBW PRIMARY FLIGHT CONTROL SYSTEM

It has three operating modes: Normal, Secondary, and Direct.

- ## NORMAL

In this mode the PFCs supply actuator position commands to the ACEs, which convert them into an analog servo command. Full functionality is provided, including all enhanced performance, envelope protection, and ride quality features.

- ## SECONDARY

In this mode, the PFCs supply actuator position commands to the ACEs, just as in the "Normal" mode. However, functionality of the system is reduced. For example, the envelope protection functions are not active in the "Secondary" mode. The PFCs enter this mode automatically from the "Normal" mode when there are sufficient failures in the system or interfacing systems such that the "Normal" mode is no longer supported. An example of a set of failures that will automatically drop the system into the "Secondary" mode is total loss of airplane air data from the ADIRU and SAARU. The airplane is quite capable of being flown for a long period of time in the "Secondary" mode.
NOTE But it cannot, however, be dispatched in this condition.

- ## DIRECT

In this mode, the ACEs do not process commands from the PFCs. Instead, each ACE decodes pilot commands directly from the pilot controller transducers and uses them for the closed loop servo control of the actuators. This mode will automatically be entered due to total failure of all three PFCs, failures internal to the ACEs, loss of the flight controls ARINC 629 data busses, or some combination of these failures. It may also be selected manually via the PFC disconnect switch on the overhead panel in the flight deck. The airplane handling characteristics in the "Direct" mode closely match those of the "Secondary" mode.

WARNING AND CAUTION IN PRIMARY FLIGHT CONTROLS SYSTEM DISPLAYS

The primary displays for the Primary Flight Control System on the Boeing are the Engine Indication and Crew Alerting System (EICAS) display and the Multi-Function Display (MFD) in the flight deck and on Airbus ECAM. Any failures that require flight crew knowledge or action are displayed on these displays in the form of an English language message. The basic rule is to get the crews attention only when an action is necessary to cope with a failure or to cope with a possible future failure. On the other hand, maintenance personnel must get all the failure information. These messages have several different levels associated with them, depending upon the level of severity of the failure.

- ## WARNING (RED WITH ALERT)

A non normal operational or airplane system condition that requires immediate crew awareness and immediate pilot corrective compensatory action (for example, to reduce airplane speed).

- ## CAUTION (AMBER WITH AURAL ALERT)

A non normal or airplane system condition that requires immediate crew awareness. Compensatory or corrective action may be required. (For example, in case of loss of flight envelope protections an airplane speed should not be exceeded).

- ## ADVISORY (AMBER WITH NO AURAL ALERT)

A non normal operational or airplane system condition which requires crew awareness. Compensatory or corrective action may be required.

- ## STATUS (WHITE)

No Dispatch or Minimum Equipment List (MEL) related items requiring crew awareness prior to dispatch. Also available on the MFD, but not normally displayed in flight, is the flight control synoptic page, which shows the position of all the flight control surfaces.

NOTE

Priority rules among these warnings and cautions are defined to present the most important message first.

MAINTENANCE

For display and control, CMC (Central Maintenance Computer) uses Maintenance Access Terminal (MAT) and to load new software, CMC can use the Data Loader function on the MAT. This Permits PFCs to update a new software configuration without having to take them out of service. The main interface to the Primary Flight Control System for the line mechanic is the Central Maintenance Computer (CMC) function of AIMS.

ROLE OF THE CMC

To identify failures present in the system and to assist in their repair.

FEATURES

The two features utilized by the CMC that accomplish these tasks are:

- ## MAINTENANCE MESSAGES

Maintenance messages describe to the mechanic, in simplified English, what failures are present in the system and the components possibly at fault.

- ## GROUND MAINTENANCE TESTS

The ground maintenance tests exercise the system, test for active and latent failures, and confirm any repair action taken. They are also used to unlatch any EICAS and Maintenance Messages that may have become latched due to failures. All the major components of the system are Line Replaceable Units (LRU). This includes all electronics modules, ARINC 629 data bus couplers, hydraulic and electrical actuators, and all position, force, and pressure transducers. The major LRUs of the system (transducers, actuators, and electronics modules) have LRU Replacement Tests that are able to be selected via a MAT pull- down menu and are run by the PFCs. Any failures found in an LRU replacement test will result in a maintenance message, which details the failures that are present.

FLIGHT CONTROLS DIRECT CURRENT (FCDC) POWER SYSTEM

The three individual power systems dedicated to the Primary Flight Control System, which are collectively referred to as the FCDC. An FCDC Power Supply Assembly (PSA) powers each of the three power systems. Two dedicated Permanent Magnet Generators (PMG) on each engine generate AC power for the FCDC power system.

Each PSA converts the PMG alternating current into 28 V DC for use by the electronic modules in the Primary Flight Control System. Alternative power sources for the PSAs include the airplane Ram Air Turbine (RAT), the 28-V DC main airplane busses, the airplane hot battery buss, and dedicated 5 Ah FCDC batteries. During flight, the PSAs draw power from the PMGs. For on-ground engines-off operation or for in-flight failures of the PMGs, the PSAs draw power from any available source. The control surfaces on the wing and tail of Typical Aircraft is controlled by hydraulically powered, electrically signaled actuators. The elevators, ailerons, and flaperons are controlled by two actuators per surface the rudder is controlled by three. Each spoiler panel is powered by a single actuator. The horizontal stabilizer is positioned by two parallel hydraulic motors driving the stabilizer jackscrew.

ACTUATION

The actuation and powering of elevators, ailerons, flaperons, and rudder in several operational modes. These modes, defined below.

- ## ACTIVE

Normally, all the actuators on the elevators, ailerons, flaperons, and rudder receive commands from their respective ACEs and position the surfaces accordingly. The actuators will remain in the active mode until commanded into another mode by the ACEs.

- ## BY PASSED

In this mode, the actuator does not respond to commands from its ACE. The actuator is allowed to move freely, so that the redundant actuator(s) on a given surface may position the surface without any loss of authority, i.e., the actuator in the active mode does not have to overpower the bypassed actuator. This mode is present on the aileron, flaperon, and rudder actuators.

- ## DAMPED

In this mode, the actuator does not respond to the commands from the ACE. The actuator is allowed to move, but at a restricted rate which provides flutter damping for that surface. This mode allows

the other actuator(s) on the surface to continue to operate the surface at a rate sufficient for airplane control. This mode is present on elevator and rudder actuators.

- BLOCKED

In this mode, the actuator does not respond to commands from the ACE, and it is not allowed to move. When both actuators on a surface (which is controlled by two actuators) have failed, they both enter the ''Blocked'' mode. This provides a hydraulic lock on the surface. This mode is present on the elevator and aileron actuators.
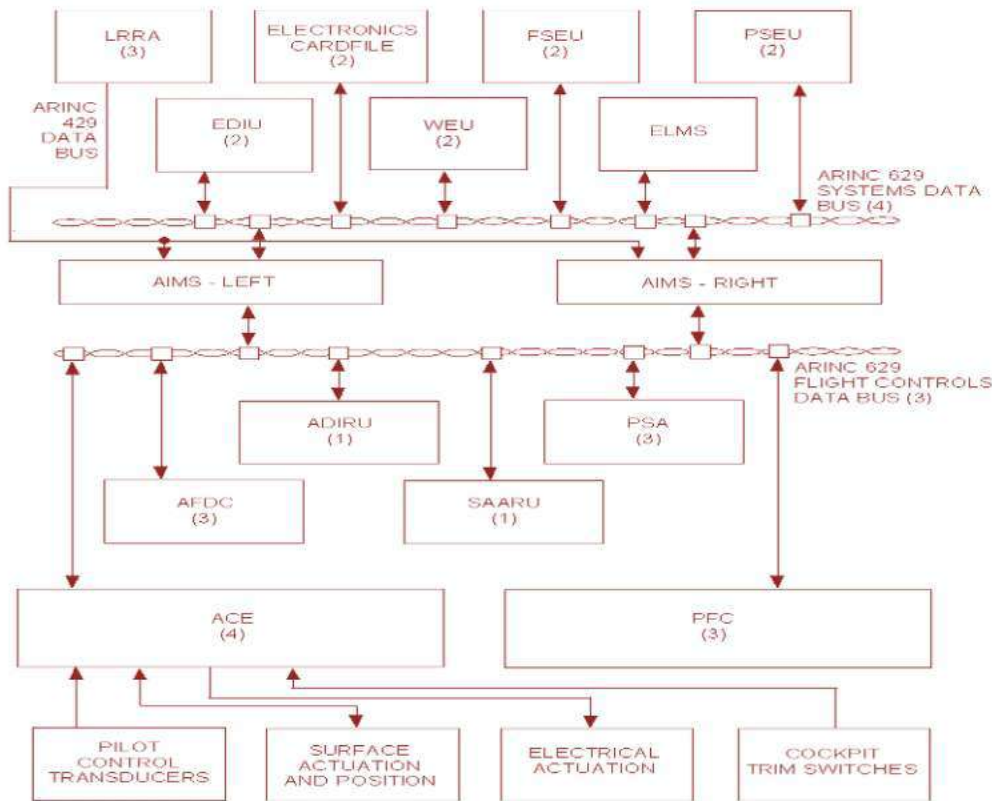
Figure 15.10: Block diagram of the electronic components of Primary Flight Control System, as well as the interfaces to other airplane systems

FLIGHT MANAGEMENT SYSTEM

The FMS provides the primary navigation, flight planning, and optimized route determination and enroute guidance for the aircraft and is typically comprised of the following interrelated functions: navigation, flight planning, trajectory prediction, performance computations, and guidance. To accomplish these functions the FMS must interface with several other avionics systems.

The FMS typically consists of two units, a computer unit and a control display unit.

1. THE COMPUTER UNIT

It can be a standalone unit providing both the computing platform and various interfaces to other avionics or it can be integrated as a function on a hardware platform such as an Integrated Modular Avionics cabinet (IMA).

2. THE CONTROL DISPLAY UNIT (CDU OR MCDU)

It provides the primary human/machine interface for data entry and information display. With its current role in the aircraft, the flight management system becomes a primary player in the current and future CNS/ATM environment. Navigation within RNP airspace, data-linked clearances and weather, aircraft trajectory-based traffic management, time navigation for aircraft flow control, and seamless low-visibility approach guidance all are enabled through advanced flight management functionality.

At the center of the FMS functionality is the flight plan construction and subsequent construction of the four-dimensional aircraft trajectory defined by the specified flight plan legs and constraints and the aircraft performance. Flight plan and trajectory prediction work together to produce the four-dimensional trajectory and consolidate all the relevant trajectory information into a flight plan/profile buffer. The navigation function provides the dynamic current aircraft state to the other functions. The vertical, lateral steering, and performance advisory functions use the current aircraft state from navigation and the information in the flight plan/profile buffer to provide guidance, reference, and advisory information relative to the defined trajectory and aircraft state.

FMS FUNCTION

- **THE NAVIGATION FUNCTION**
Responsible for determining the best estimate of the current state of the aircraft.

- **THE FLIGHT PLANNING FUNCTION**
Allows the crew to establish a routing for the aircraft.

- **THE TRAJECTORY PREDICTION FUNCTION**
Responsible for computing the predicted aircraft profile along the entire specified routing.

- **THE PERFORMANCE FUNCTION**
Provides the crew with aircraft unique performance information such as takeoff speeds, altitude capability, and profile optimization advisories.

- **THE GUIDANCE FUNCTIONS**
Responsible for producing commands to guide the aircraft along both the lateral and vertical computed profiles. Depending on the particular implementation, the ancillary I/O, BITE, and control display functions may be included as well. There are typically two loadable databases that support the core flight management functions :
- The navigation database which must be updated on a monthly cycle and
- The performance database that only gets updated if there's been a change in the aircraft performance characteristics (i.e., engine variants or structural variants affecting the drag of the aircraft).

- The navigation database contains published data relating to airports, nav aids, named waypoints, airways and terminal area procedures along with RNP values specified for the associated airspace. The purpose of the navigation data base is twofold. It provides the navigation function location, frequency, elevation, and class information for the various ground-based radio navigation systems. This information is necessary to select, auto- tune, and process the data from the navigation radios (distance, bearing, or path deviation) into an aircraft position. It also

Provides the flight plan function with airport, airport-specific arrival, departure, and approach procedures (predefined strings of terminal area waypoints), airways (predefined en route waypoint strings), and named waypoint information that allows for rapid route construction.
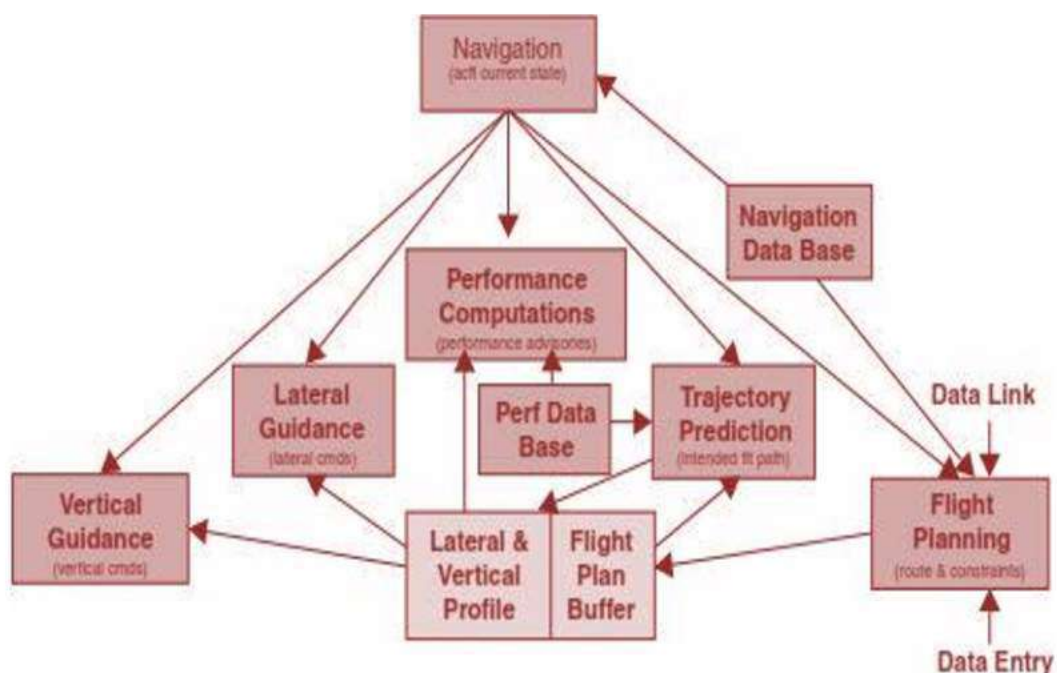
Figure 15.11

THE FUNCTION OF NAVIGATION IN FMS

To computes aircraft current state based on a statistical blending of multi sensor position and velocity data. The navigation function is designed to operate with various combinations of autonomous sensors and navigation receivers. The position update information from the navigation receivers is used to calibrate the position and velocity data from the autonomous sensors, in effect providing an error model for the autonomous sensors.

The current state data of aircraft usually includes:
- Three-dimensional position (latitude, longitude, altitude)
- Velocity vector
- Altitude rate
- Track angle, heading, and drift angle
- Wind vector

- Estimated Position Uncertainty (EPU)
- Time

A TYPICAL NAVIGATION SENSORS ARE:

1. AUTONOMOUS SENSORS
   - Inertial reference
   - Air data

   - ## NAVIGATION RECEIVERS
   - DME receivers
   - VOR/LOC receivers
   - GPS receivers

   - ## NAVIGATION PERFORMANCE

- The navigation function, to be RNP airspace compliant per DO- 236, must compute an Estimated Position Uncertainty (EPU) that represents the 95% accuracy performance of the navigation solution. The EPU is computed based on the error characteristics of the particular sensors being used and the variance of the individual sensors position with respect to other sensors. The RNP for the airspace is defined as the minimum navigation performance required for operation within that airspace. It is specified by default values based on the flight phase retrieved from the navigation data base for selected flight legs or crew entered in response to ATC-determined airspace usage. A warning is issued to the crew if the EPU grows larger than the RNP required for operation within the airspace. The table below shows the current default RNP values for the various airspace categories.
2. A pictorial depiction of the EPU computation is shown below for a VOR/VOR position solution. A similar representation could be drawn for other sensors. As can be seen from the diagram, the estimated position uncertainty (EPU) is dependent on the error characteristics of the particular navigation system being used as well as the geometric positioning of the nav aids themselves. Other navigation sensors such as an inertial reference system have error characteristics that are time-dependent. More information pertaining to EPU and various navigation nav aid system error characteristics can be found in RTCA DO-236.

1. GLOBAL POSITIONING SYSTEM (GPS)

The GPS receiver is self-managing in that the FMS receives position, velocity, and time information without any particular FMS commands or processing. In ARINC 743 detailed informations on the GPS interface and function can be found.

2. VHF NAVAIDS (DME / VOR / ILS)

The DME/VOR/ILS receivers must be tuned to an appropriate station to receive data. The crew may manually tune these receivers but the FMS navigation function will also auto-tune the receivers by

selecting an appropriate set of stations from its stored navigation database and sending tuning commands to the receiver(s).

Since DMEs receive ranging data and VORs receive bearing data from the fixed station location, the stations must be paired to determine a position solution as shown below:

The pairing of navaids to obtain a position fix is based on the best geometry to minimize the position uncertainty (minimize the portion of EPU caused by geometric dilution of precision, GDOP). As can be seen from the figure above, the FMS navigation must process range data from DMEs and bearing data from VORs to compute an estimated aircraft position. Further, since the DME receives slant range data from ground station to aircraft, the FMS must first correct the slant range data for station elevation and aircraft altitude to compute the actual ground-

projected range used to determine position. The station position, elevation, declination, and class are all stored as part of the FMS navigation data base. There are variations in the station-tuning capabilities of DME receivers. A standard DME can only accept one tuning command at a time, an agility-capable DME can accept two tuning commands at a time, and a scanning DME can accept up to five tuning commands at a time. VOR receivers can only accept one tuning command at a time.

An ILS or LOC receiver works somewhat differently in that it receives cross-track deviation information referenced to a known path into a ground station position. These facilities are utilized as landing aids and therefore are located near runways. The FMS navigation function processes the cross-track information to update the cross-track component of its estimated position as shown in figure 15.12. More Information about DME/VOR/ILS can be found in ARINC709, 711, and 710, respectively.
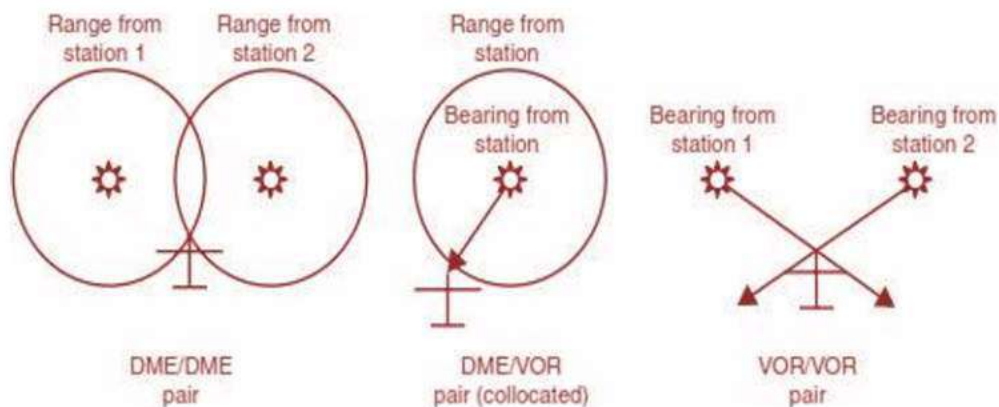

Figure 15.12

FLIGHT PLANNING

It is the route in which aircraft is to fly from the departure airport to the destination airport. Route data are typically extracted from the FMC (Flight Management computer) navigation data base and typically consists of :

- A departure airport and runway
- A standard instrument departure (SID) procedure

- A standard arrival (STAR) procedure, and an approach procedure with a specific destination runway. Often the estimation arrival (or approach transition) and approach procedure are not selected until the destination terminal area control is contacted.
- En route waypoints and Airways.

The selection of flight planning data is done by the crew through menu selections either on the MCDU or navigation display or by data link from the airline's operational control. Some of the methods for the crew to create new fixes (waypoints) are listed below.

1. LAT / LON CROSSING WAYPOINTS

Created by specifying a latitude or longitude. A waypoint will be created where the active flight plan crosses that latitude or longitude. Latitude or longitude increments can also be specified, in which case several waypoints are created where the flight plan crosses the specified increments of latitude or longitude.

2. INTERSECTION OF AIRWAYS

Created by specifying two airways. A waypoint will be created at the first point where the airways cross.

3. FIX WAYPOINTS

Created by specifying a "fix" reference. Reference information includes creation of a beam waypoints and creation of waypoints where the intersections of a specified radial or distance from the "fix" intersects the current flight plan.

4. RUNWAY EXTENSION WAYPOINTS

Created by specifying a distance from a given runway. The new waypoint will be located that distance from the runway threshold along the runway heading.

CONSTRUCTION OF FLIGHT PLAN

They are constructed by linking data stored in the navigation data base. The data may include any combination of the following items:
1. SID/STAR/approach procedures
2. Airways
3. Pre stored company routes
4. Fixes (en route waypoints, nav aids, non directional beacons, terminal waypoints, airport reference points, runway thresholds)
5. Crew-defined fixes

Terminal area procedures (SIDs, STARs, and approaches) consist of a variety of special procedure legs and waypoints. Procedure legs are generally defined by a leg heading, course or track, and a leg termination type. The termination type can be specified in many ways such as an altitude, a distance, or intercept of another leg.

PERFORMANCE COMPUTATIONS

The performance function provides the crew information to help optimize the flight or provide performance information that would otherwise have to be ascertained from the aircraft performance manual. FMSs implement a variety of these workload reduction features.

GUIDANCE

The FMS typically computes roll axis, pitch axis, and thrust axis commands to guide the aircraft to the computed lateral and vertical profiles. These commands may change forms depending on the particular flight controls equipment installed on a given aircraft. Other guidance information is sent to the forward field of view displays in the form of lateral and vertical path information, path deviations, target speeds, thrust limits and targets, and command mode information.

LATERAL GUIDANCE

The lateral guidance function typically computes dynamic guidance data based on the predicted lateral profile. The data are comprised of the classic horizontal situation information:
- Distance to go to the active lateral waypoint (DTG)
- Desired track (DTRK)
- Track angle error (TRKERR)
- Cross-track error (XTRK)
- Drift angle (DA)
- Bearing to the go to waypoint (BRG)
- Lateral track change alert (LNAV alert)

VERTICAL GUIDANCE

The vertical guidance function provides commands of pitch, pitch rate, and thrust control to the parameters of target speeds, target thrusts, target altitudes, and target vertical speeds (some FMS provide only the targets depending on the flight management / flight control architecture of the particular aircraft). Much like the lateral guidance function, the vertical guidance function provides dynamic guidance parameters for the active vertical leg to provide the crew with vertical situation awareness. Unlike the lateral guidance parameters, the vertical guidance parameters are somewhat flight phase dependent.

Vertical guidance is based on the vertical profile computed by the trajectory prediction function as described in a previous section as well as performance algorithms driven by data from the performance data base.

BITE MAINTENANCE OF FMS

The flight controls maintenance and failure detection function is built around the 2 Flight Control Data Concentrators (FCDC's). The failure detection is ensured by the Flight Control Primary Computers (FCPC's), Flight Control Secondary Computers (FCSC's) and FCDC's. The FCPC's and FCSC's send failure information to the FCDC's which analyse, store them and send maintenance messages to the Central Maintenance Computers (CMC's). The failure data are accessible on the Multipurpose Control and Display Unit (MCDU) in the form of maintenance messages.

TESTS IN INTERACTIVE MODE

The electrical flight control system comprises 5 tests initiated on the ground from the MCDU. These tests are managed by the FCDC's:

- System test
- Elevator servo control damping test
- Inboard aileron servo control damping test
- Outboard aileron servo control damping test
- Back-Up Yaw Damper test.

AUTOMATIC TESTS

Two types of automatic tests are built in the flight control computers:

- The power-up tests
- The automatic tests performed at engine start availability of stand-by control channels.

INTERFACE

- Interface between the FCPC's, FCSC's and FCDC's
- Interface with the Onboard Maintenance System (OMS) The link between the CMC and the FCDC's is ensured by ARINC 429 buses; and is bi-directional
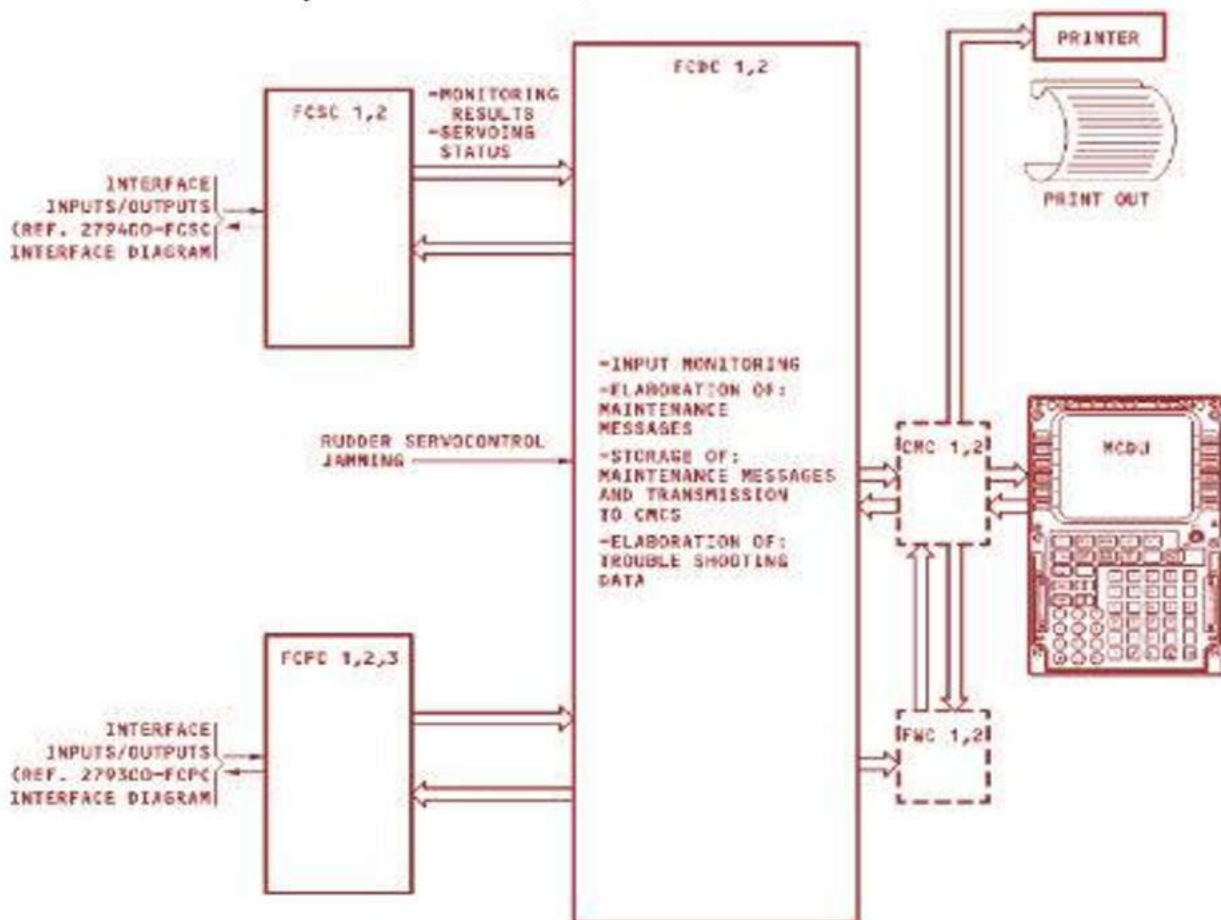

Figure 15.13: Test Equipment of the EFCS System

FAILURE DETECTION

Except for the rudder servo control jamming detection which is ensured by the FCDC's, failure detection of the other LRU's is ensured by the FCPC's and FC-SC's at the time of input validation by the monitoring related to serving and the computer internal monitoring. When a failure is detected:

- The FCPC's and FCSC's take operational actions (system reconfiguration) and send failure information to the FCDC's.
- From this primary failure information (loss of serving, etc.); the FCDC's elaborate a warning Boolean and if necessary the complementary data required to animate the ECAM System page.
- Moreover, the FCDC's analyse the failure and, after confirmation, generate a maintenance message. The message gives in clear language the designation, FIN and ATA chapter related to the removal of the concerned LRU. This message is permanently transmitted to the CMC's.
- The FCDC's memorize the message and associate the time, date of failure occurrence and additional data linked to the failure.
- The memorization is performed in the FCDC 1 and 2 as per the rules below:
    - ✓ The system failures (ATA 27 except SLAT/FLAP system) are considered as internal failures.
    - ✓ The others (e.g. ADIRU failures) are considered as external failures.
    - ✓ The transmission is performed as per the rules below:
    - ✓ If both FCDC's are available, FCDC 1 sends external and internal failures while the FCDC 2 sends all failures as external to avoid double storage within the CMC.

- If the FCDC 1 is not available, the FCDC 2 sends failures classified as internal and external.

BUILT IN TEST EQUIPMENT (BITE) INTRODUCTION

In most modern aircraft such as Airbus A320, A330, A340 and Boeing 747-300, Boeing 777 and MD11, Onboard Maintenance Systems are installed and during normal operation, the system is permanently monitored: internal monitoring, inputs/ outputs monitoring, link monitoring between LRU's within the system.

Onboard Maintenance Systems collect failure reports from each system computer BITE and shows the failures on a display in the cockpit or allows printing of the failures on an onboard printer. System Tests or Return to Service Tests can be initiated from a maintenance device in the cockpit. A system is composed of LRU's which can be: computers, sensors, actuators, probes, etc. With the new technology, most of these Line Replaceable Units (LRU's) are controlled by digital computers. For safety reasons, these LRU's are permanently monitored, they can be tested and troubleshooting can be per formed. In each system, a part of a computer is dedicated to these functions: it is called Built- In Test Equipment. Sometimes, in multi- computer systems, one computer is used to concentrate the BITE (Built- In Test Equipment) data of system. In this graphic below, all the indicating/recording systems can be seen together.

CENTRALIZED FAULT DISPLAY SYSTEM

The Centralized Fault Display Interface Unit (CFDIU) centralizes and memorizes all information concerning A/C system failures. Reading or printing of the failure information is done in the cockpit with any MCDU or the printer. Most A/C system computers have a BITE. The BITE permanently monitors the system operation. When a failure is detected, it is stored in the BITE memory and is transmitted to the CFDIU. The ECAM also monitors the A/C systems. The warning information is delivered to the CFDIU. The failure information is available in various reports. The reading of the failure information is made from two different MCDU menus depending on if the A/C is in flight or on ground. The SYSTEM REPORT/TEST function is available on ground only. It enables a dialogue between the CFDIU and a system computer. The SYSTEM REPORT/TEST menu page presents the list of all the systems connected to the CFDIU, in ATA chapter order. The maintenance Post Flight Report (PFR) can only be printed on ground. It summarizes and displays the list of the ECAM warning messages and the fault messages that occurred during the last flight, with the associated time, flight phase and ATA reference. It helps the maintenance crew to make a correlation for easier troubleshooting.

MAINTENANCE / TEST FACILITIES

All the navigation systems can be tested from the MCDUs. ISIS additional tests and other data are available from its display front face.

FAULT DETECTION

If a failure occurs, it can be permanent (consolidated) or intermittent.

ISOLATION

After failure detection, the BITE is able to identify the possible failed LRU's and can give a snapshot of the system environment when the failure occurred.

MEMORIZATION

All the information necessary for maintenance and trouble shooting is memorized in a Non Volatile Memory.
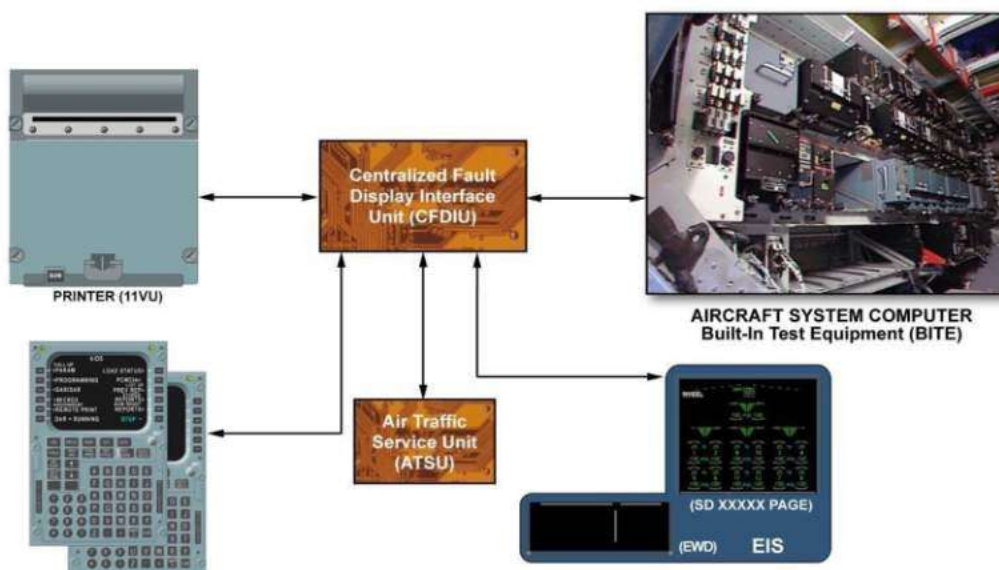

Figure 15.14: Typical Centralized Fault Display System

The test function can be divided into 4 groups.

POWER UP TEST

The power up test is first a safety test. The purpose of a safety test is to ensure compliance with the safety objectives. It is executed only on ground after long power cuts (more than 200 ms). Its duration is function of the system which is not operational during the power up test. If the aircraft is airborne, the power up test is limited to a few items to enable a quick return to operation of the system. The typical tasks of a power up test are: test of microprocessor, test of memories, test of ARINC 429 and various I/O circuits, configuration test.

CYCLIC TESTS

These tests are carried out permanently. They do not disturb system operation. The typical tasks of a cyclic test (also called IN OPERATION TEST) are:
Watch-dog test (a watchdog is a device capable of restarting the microprocessor if the software fails), RAM test. Permanent monitoring is performed by the operational program (e.g. ARINC 429 messages validity).

SYSTEM TEST

The purpose of this test is to offer to the maintenance staff the possibility to test the system for trouble shooting purposes. This test can be performed after the replacement of a LRU in order to check the integrity of the system or sub-system. It is similar to the POWER UP TEST but it is more complete. It is performed with all peripherals supplied.

SPECIFIC TESTS

For some systems, specific tests are available. The purpose of these tests is to generate stimuli to various command devices such as actuators or valves. They can have a major effect on the aircraft (automatic moving of slats or flaps, engine dry cranking).

NEW CONCEPT

The BITE information stored in the system BITE memories is sent to a centralized maintenance device. The manual tests (SYSTEM TEST and SPECIFIC TESTS) can be initiated via this centralized maintenance device. Its main advantages are:

- Single interface location (cockpit).
- Easy fault identification.
- Reduction of the trouble shooting duration.
- Simplification of the technical documentation.
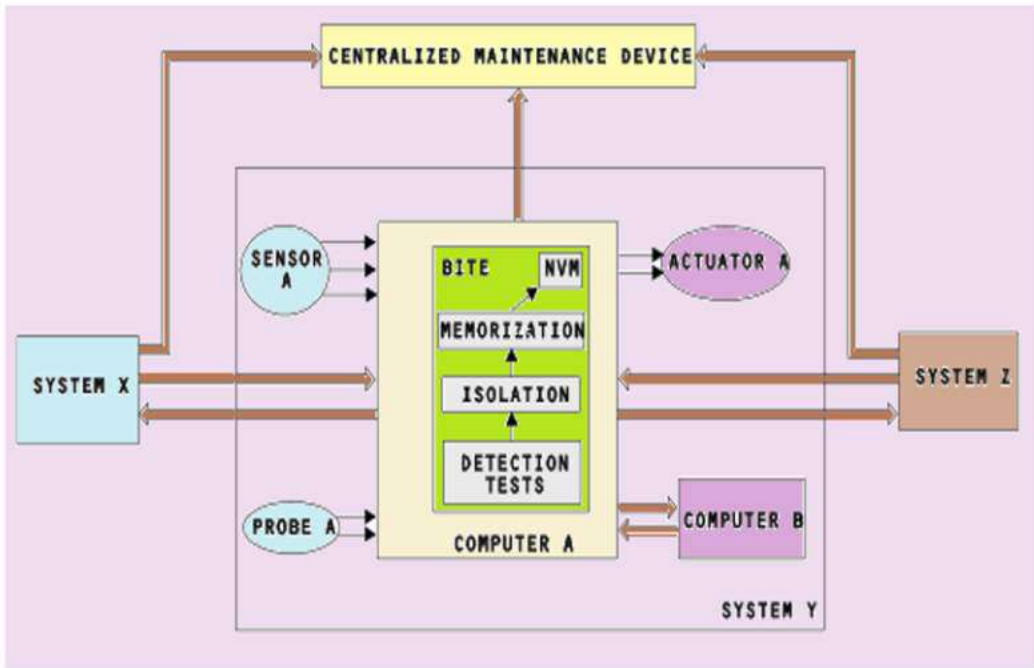- Standardization of the equipment.
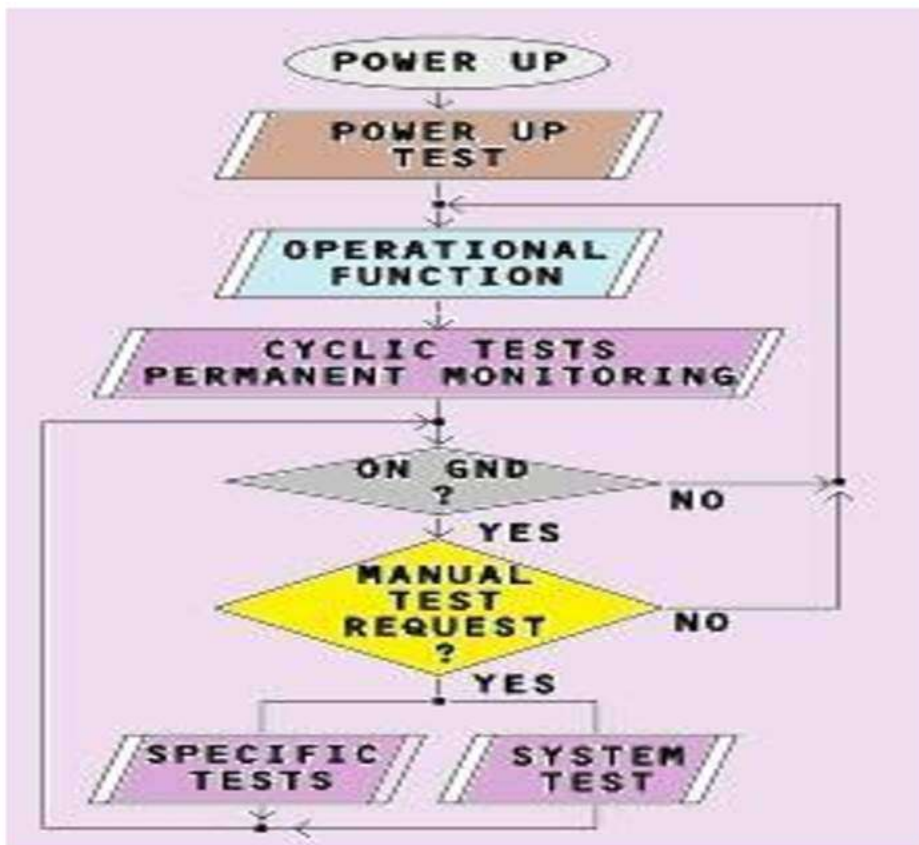
Figure 15.15 (a): BITE Philosophy

Figure 15.15 (b): Computer Software Process

BITE TESTING OF THE EIS SYSTEM MAINTENANCE AND TEST

The EIS includes Hard-oriented and Soft-oriented Built-In-Test (BITE) functions. The CFDS (Centralized Fault Data System) facilitates the interface of these BITE resident routines for maintenance and test implemented in the various computers Failure Detection Functions: The BITE of a computer is able to detect the internal failures as well as failures affecting the I/P parameters. The BITE is designed so as to minimize the undetected failures, and to make the maintenance of the system easier. To that end, the events detected by the BITE (anomaly, abnormal disengagement, failure...) are coded and stored in non- volatile memories called BITE memories, under the form of messages in alphanumeric characters. The GMT at the time of each failure is recorded and stored with the associated event. The BITE memories store information concerning several flights. The CFDS helps the flight crew and the maintenance personnel by providing the capability of displaying the above messages, as well as system maintenance data and procedures, through the interactive Multipurpose Control and Display Units (MCDU's), located on the center pedestal.
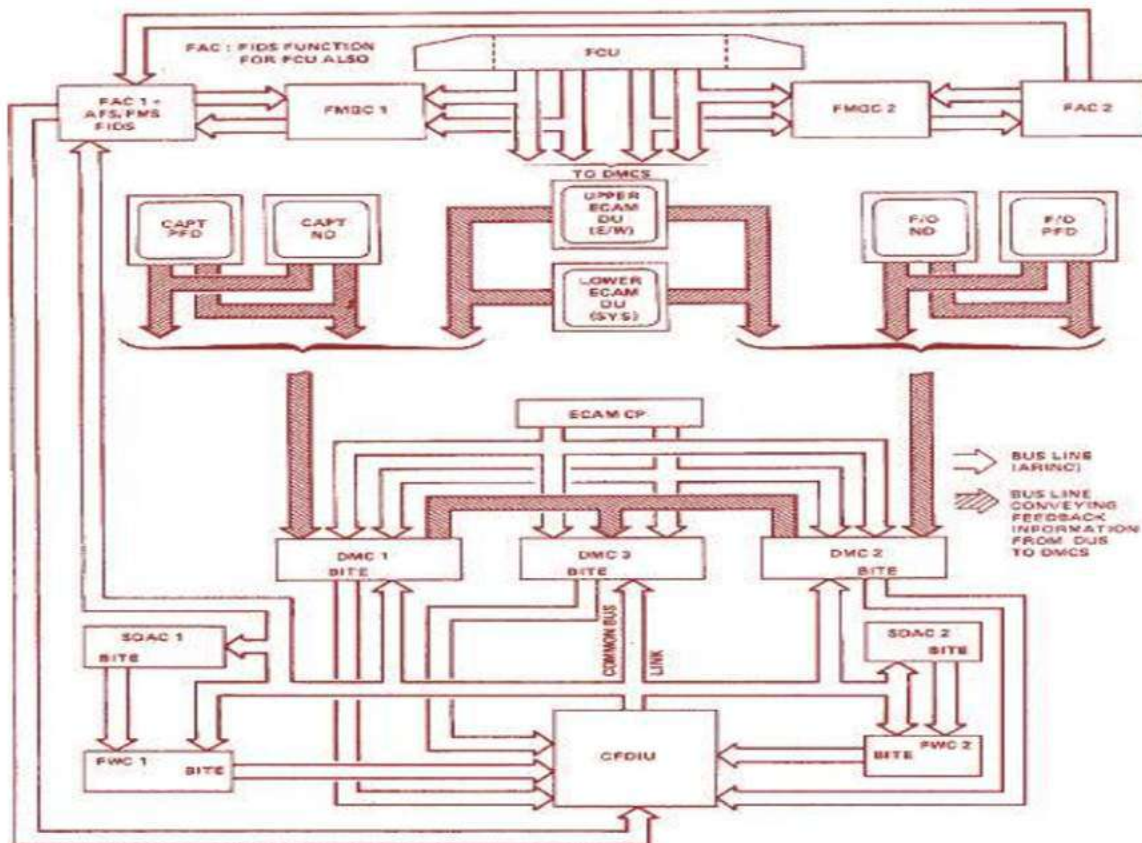

Figure 15.16: BITE Connections of the EIS System

BITE TESTING OF THE ATIMS SYSTEM

The Basic ATSU interface software enables the BITE testing of the ATIMS system. Testing is done using the MCDU in the Cockpit. A specific menu on the MCDU gives access to the Test function.

Failures of the system components are then collected and reported as Test Result, if no failures are present, a Test OK. Message will be displayed.

EIS ABNORMAL OPERATION

1. FAILURE OF THE ENGINE/WARNING DISPLAY UNIT

The Engine/Warning Display (EWD) has priority over the System Display (SD). The EWD is automatically transferred to the lower Electronic Centralized Aircraft Monitoring (ECAM) DU, replacing the system/status display. All ECAM information and system/status pages are available on this single display. This configuration is called "ECAM mono display".

Figure 15.17: Failure of the Engine / Warning Display Unit

2. FAILURE OF BOTH ECAM DISPLAY UNITS

ECAM / ND transfer (XFR) is done to get the engine/warning image back. All the ECAM images are lost momentarily. However the crew can recover the engine/warning image by using the ECAM / ND XFR rotary selector. The engine/warning image will then be displayed instead of the ND. This configuration is called "ECAM mono display" because all ECAM information is Available on a single display.
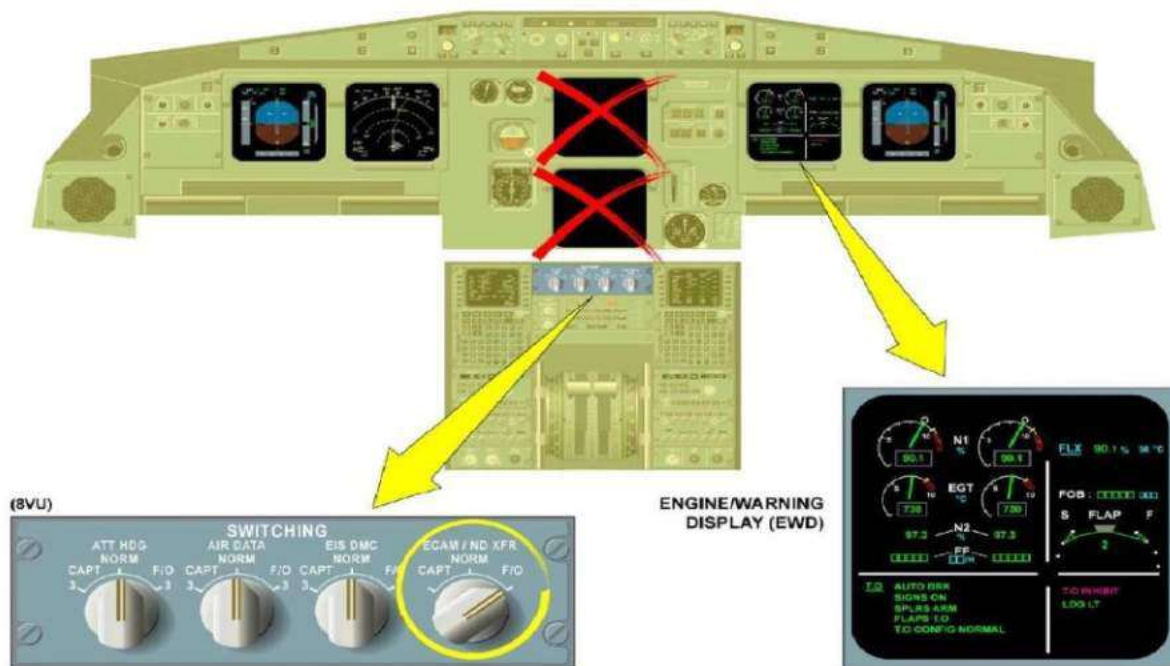
Figure 15.18: Failure of Both ECAM Display Units

AUTOMATIC TEST EQUIPMENT (ATE)

ATE is a dedicated ground test instrument that provides a variety of different tests and functional checks on an LRU or printed circuit card. By making a large number of simultaneous connections with the equipment under test, ATE is able to gather a large amount of data very quickly, thus avoiding the need to make a very large number of manual measurements in order to assess the functional status of an item of equipment. ATE systems tend to be dedicated to a particular avionic system and are expensive to develop and manufacture. Because of this they tend to be only used by original equipment manufacturers (OEM) and licensed repairers. ATE systems usually incorporate computer controls with displays that indicate what further action (repair or adjustment) is necessary in order maintain the equipment. Finally, it is worth noting that, individual items of equipment may often require further detailed tests and measurements following initial diagnosis using ATE.

Figure 15.19: ECAM cockpit print out showing warning and failure messages

GLOBAL POSITIONING SYSTEM (GPS)

The Global Positioning System (GPS) provides the following positional information on a worldwide basis. The information
Can comprise:

- Latitude
- Longitude
- Altitude
- Time
- Speed

GPS provides highly accurate navigational information. The system is based on 24 satellites in six orbits with four satellites per orbit. GPS was a spin off from two experimental satellite navigation programmes carried out by the US Navy and Air Force and tended to facilitate precision aimed weapons and accurate troop deployment. Although the system is now available to the civilian market, it is still controlled and administered by the US Department of Defence. The system is highly accurate although, should the need arise, the US military can degrade the accuracy of the system to suit (up to 1,000 m). The main advantages of GPS are:

- Accuracy
- Global application
- Signal fidelity

Very precisely positioned orbiting satellites transmit very accurate, coded satellite position and time data. The receiver decodes this data and calculates its position relative to the satellite. If the receiver is moving then these characteristics must be included for accurate results. Using data from more than one satellite improves accuracy. The accuracy is ultimately based on very precise atomic clocks in each satellite. GPS consists of three segments; the Space Segment, the User Segment and the Control Segment. We shall briefly explain each of these in turn.

SPACE SEGMENT

The Space Segment consists of a minimum of 24 operational satellites in six circular orbits 20,200 km (10,900 nm) above the earth at an inclination angle of 55 degrees with a 12 hour period. The satellites are spaced in orbit so that at any time a minimum of six satellites will be in view to users anywhere in the world (see Fig.-15.20). The satellites (see Fig-15.21) continuously broadcast position and time data to users throughout the world. Transmission accuracy is maintained using atomic clocks accurate to within 0.1 s in 10,000 years. System accuracy is dependent on the perfect synchronisation of receiver and satellite clocks and the quality of the receiver clock. Note that using data from several satellites can help to reduce these errors.

USER SEGMENT

The User Segment consists of the receivers, processors, and antennas that allow land, sea, or airborne operators to receive the GPS satellite broadcasts and compute their precise position, velocity and time.

CONTROL SEGMENT

The Control Segment consists of a master control station in Colorado Springs, with five monitor stations and three ground antennas located throughout the world. The monitor stations track all GPS satellites in view and collect ranging information from the satellite broadcasts. The monitor stations send the information they collect from each of the satellites back to the master control station, which computes extremely precise satellite orbits. The information is then formatted into updated navigation messages for each satellite. The updated information is transmitted to each satellite via the ground antennas, which also transmit and receive satellite control and monitoring signals.
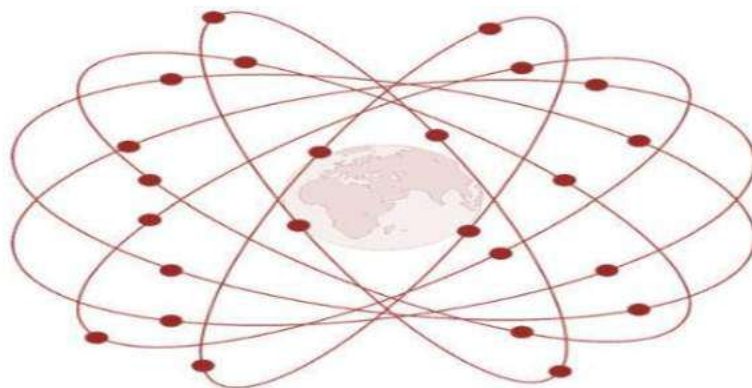
GPS uses 24 satellites in six orbital planes (there are four satellites in each plane)

Fig.-15.20

A Navstar GPS satellite under construction

Figure 15.21

GPS FREQUENCIES

Each satellite transmits two carriers; L1 at 1,575.42 MHz and L2 at 1,227.60 MHz. The L1 signal is modulated by a 1.023 MHz coarse / acquisition code (C/A) that repeats every 1 ms. Although the coded signal is repetitive is appears as random and is called Pseudo Random Noise (PRN). The L2

carrier is modulated by another apparently random coded PRN signal at 10.23 MHz. This signal is known as the Precision (P) code and it repeats every 267 days. Each satellite is allocated a unique seven day segment of this code. A third signal containing navigation data is superimposed on each already complex signal containing the satellite status, ephemeris data, clock error and tropospheric and ionospheric data for error correction. Interestingly, the US control section can 'dither' these frequencies at any time to invalidate any known codes thus making the GPS inoperative to those without knowledge of this dither coding. When this is done the code is know as the Y code and is only suitable for military / political applications. With the exception of Y coding each PS receiver knows the modulation codes for each satellite and it is simply a matter of decoding the received signals to identify the satellite and then removing the carrier from the received signals to extract the navigation data.

DESCRIPTION AND OPERATION

The Multi Mode Receiver (MMR) receives RF signals through an active GPS antenna (preamplifier implemented within the antenna). The GPS receiver filters, mixes, and performs analog-to- digital conversions. The resulting data is processed by microprocessors that output position, velocity, time, and integrity data to the system processor. The system processor transmits ARINC 743A - compliant data for use by other aircraft systems.

The GPS receiver also outputs a time mark discrete signal that tells users of the ARINC 743A data the instant in time when the position solution is valid.

ADIRU

In normal operation, the MMR1 data is used by ADIRU 1 and 3; the MMR 2 data by ADIRU 2. In order to reduce GPS Receiver initialization time, ADIRU1 and 2 respectively send data to MMR 1 and 2 (IR position, Altitude, Date, UTC).
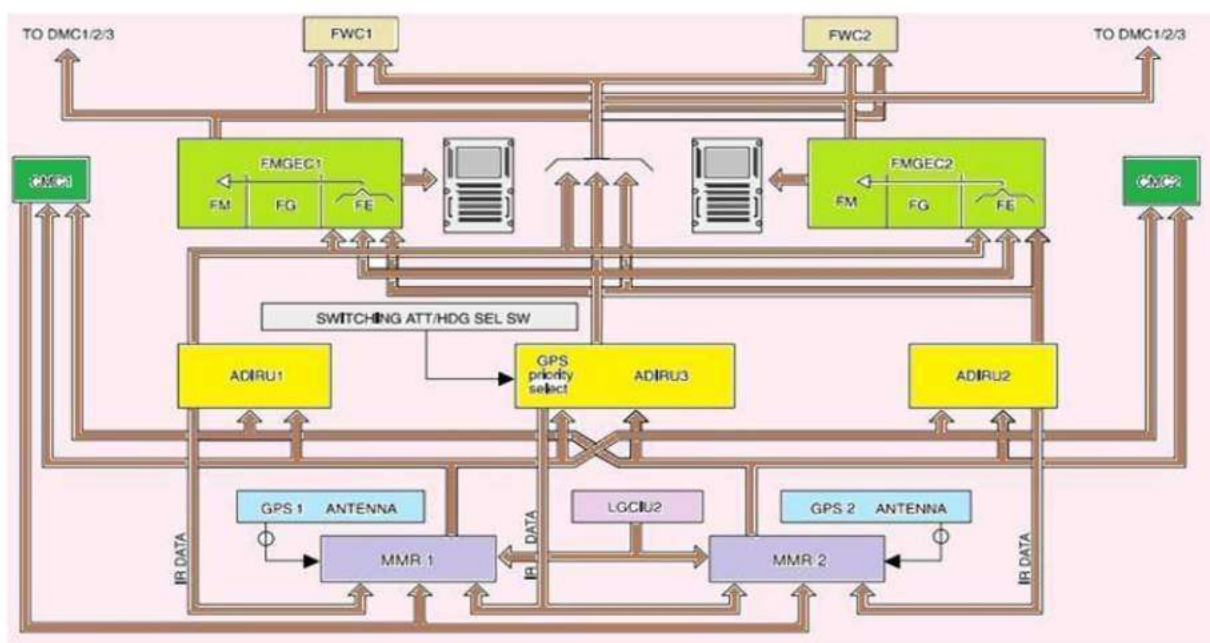

Figure 15.22 : GPS System Overview

FMGEC

The Inertial Reference portions of ADIRU 1 and 2 respectively provide Flight Management Guidance and Envelope Computer (FMGEC) 1 and 2 with pure inertial reference data, hybrid GP inertial reference data used by the FMGEC for position fixing purposes and pure GPS data which is displayed on MCDU; in this case the ADIRU operates as a relay. In case of failure of one GPS: the two ADIRU's automatically selecting the only operative GPS to compute hybrid GPIR data.

ATT / HDG SWITCHING

In case of failure of ADIRU 1, FMGEC 1 uses ADIRU 3 / GPS 1 data and in case of failure ADIRU 2, FMGEC 2 uses ADIRU 3 / GPS 2 data. The primary source of ADIRU 3 being GPS 1, it is necessary to select the secondary input part of ADIRU 3 (GPS2) by means of the SWITCHING ATT/ HDG selector switch to preserve side 1 /side 2 segregation (GPS1/ ADIRU1/ FMGEC1 and GPS2/ ADIRU3/ FMGEC2 architecture). The MMR's are monitored by the three ADIRU's using the status word send by each MMR and the BITE of the inertial reference portion.

DMC / FWC

In case of GPS failure, the NAVGPS 1(2) FAULT message is displayed on the lower part of the Engine/ Warning Display (EWD).
This message is accompanied by:
- Activation of the MASTER CAUTION lights on the glare shield,
- Aural warning: Single Chime (SC). The GPS data is displayed on the GPS Monitor Page of the MCDU through the FMGEC.

INDICATING

The displayed data are:
- GPS position (Lat/ Long)
- True track
- Figure of merit (in meters)
- Ground speed
- Mode

ANTENNA

The GPS antenna is a L- band preamplified antenna. The GPS antenna is designed to operate at 1575.42 MHz with a right hand circular polarization and to provide an omnidirectional upper hemispheric coverage.

CMC

The BITE of the MMR is connected to the Central Maintenance Computer (CMC). The units tested are the MMR, GPS Receiver, ILS Receiver, GPS antenna and co axial cable

LGCIU

This ground / flight information is used by the receiver BITE module to count the flight legs.

INERTIAL REFERENCE SYSTEM (IRS)

The Inertial Reference System (IRS) and Inertial Navigation System (INS) are methods of very accurate navigation that do not require any external input such as ground radio information. They are passive systems that work entirely independently of any external input, a very useful characteristic as the system cannot then be easily liable to interference. On modern aircraft the IRS is separate and supplies data to the FMC (the latter performing the navigation function). The basic IRS consists of:

- Gyroscopes
- Linear accelerometers
- A navigation computer
- A clock

Gyroscopes are instruments that sense directional deviation using the characteristics of a very fast spinning mass to resist turning. Three such spinning masses are mounted orthogonally in a structure known as a gimbal. This frame allows the three rotating 'gyros' to maintain their direction of spin during aircraft movement thereby indicating the 'sensed' changes. In aircraft they are used to sense angles of roll, pitch, and yaw. The accelerometers sense speed deviations (acceleration) along each of the axes. This three dimensional accelerometer/gyro configuration gives three orthogonal acceleration components which can be vectorially summed. Combining the gyro-sensed direction change with the summed accelerometer outputs yields the directional acceleration of the vehicle. The system clock determines the rate the navigation computer time integrates each directional acceleration in order to obtain the aircraft's velocity vector. The velocity vector is then integrated with time, to obtain the distance vector. These steps are continuously iterated throughout the navigation process giving accurate positional information. Crucial to the accuracy of the IRS is the initialisation of the system. This is the process of pre-flight gimbal and position alignment that gives a datum to measure all further in flight movement from. Basically, the gyros are 'run up' to speed, the compass heading is aligned, and the latitude and longitude of the origin are entered in the computer. Any further movement of the aircraft can be calculated against this datum. In modern avionics systems laser or optical gyros are used. These are more reliabledue to containing few moving parts. In addition to this, in commercial operations, GPS data is used to further facilitate accuracy. This of course is not operationally necessary but can provide additional valuable information.

GIMBALLED SYSTEMS

Gyros were initially located on a rotating platform connected to an outer housing via low friction gimbals. Accelerometers were attached to each gimballed gyro axis and thus were held in a fixed

orientation. Any angular motion was sensed by the rotating platform, this maintains the platform's original orientation. Pickoffs on the gimbals measure the movement of the outer body around the steady platform and the accelerometers measure the body's acceleration in the fixed inertial axes. Gimballed systems had a tendency to 'lock up' or 'topple' in certain violent or fast manoeuvres. Additionally they were mechanical/moving parts dependant. The gimballed systems primary advantage is its inherently lower error. Since its three orthogonal accelerometers are held in a fixed inertial orientation, only the vertically oriented one will be measuring gravity (and therefore experiencing gravity- related errors). In strap down systems, the accelerometers all move in three axes and each experiences potential errors due to gravity. Gimballed systems also have the advantage of simplicity of operation. The primary function of the gyro in a gimballed system is to spin and maintain a high moment of inertia, whereas strap down gyros need to actually measure the subtended angles of motion.

STRAP DOWN SYSTEMS

With fewer moving parts, strap down systems were developed using advanced computer technologies. Progress in electronics, optics and solid state technology have enabled very accurate reliable systems to be developed. Modern commercially available equipments take advantage of integrated circuit technologies. Strap down systems are fixed to the aircraft structure; the gyros detecting changes in angular rate and the accelerometers detecting changes in linear rate, both with respect to the fixed axes. These three axes are a moving frame of reference as opposed to the constant inertial frame of reference in the gimballed system. The system computer uses this data to calculate the motion with respect to an inertial frame of reference in three dimensions. The strap down system's main advantage is the simplicity of its mechanical design. Gimballed systems require complex and expensive design for its gimbals, pickoffs, and low-friction platform connections; strap down systems are entirely fixed to the body in motion and are largely solid-state in design.

TRAFFIC ALERT COLLISION AVOIDANCE SYSTEM (TCAS)

The Traffic Alert Collision Avoidance System (TCAS) is a surveillance and avoidance system that alerts aircrew if any other aircraft enter a predetermined envelope of airspace around an aircraft. It is a secondary radar facility (transmits to, receives transmissions from, other TCAS equipped aircraft). The evaluated traffic information is displayed as symbols on the ND, the Navigation Display. Note that altitude and vertical motion information is only available if the received signal comes from a mode C or mode S transponder. Otherwise the associated symbol on the ND will have no altitude information and no vertical motion arrow. As TCAS checks the other aircraft's relative distance permanently in short time intervals, it can therefore also calculate the other aircraft's closure rate relative to the own aircraft. The closure rate is the most important variable and indeed a very fail-safe key to a meaningful collision prediction. Complex, trigonometric calculations of flight paths and ground speeds are unnecessary and may also result in unreliable extrapolations. Note that heading or bearing information is not required to compute a TCAS alarm. When TCAS detects that an aircraft's distance and closure rate becomes critical, it generates aural and visual annunciations

for the pilots. If necessary, it also computes aural and visual pitch commands to resolve a conflict. If the other aircraft uses TCAS II as well, these pitch commands are coordinated with the other aircraft's pitch commands so that both aircraft don't 'escape' in the same direction. Even three aircraft can be coordinated. It is important to be aware that TCAS provides only vertical guidance, no lateral guidance. TCAS also ignores performance limitations. In other words, when flying at maximum altitudes TCAS may still generate a climb command! In addition to a transponder, various systems are required to run TCAS including:

- IRS (attitude data, vertical motion data)
- Gear position sensors (as the extended gear disturbs the lower directional antenna, bearing detection of traffic flying below the own aircraft must be inhibited)
- Radio altimeters (TCAS must know the radio height as the alarm logic varies with the height above ground)
- GPWS (overrides TCAS advisories during a wind shear or ground proximity warning). When an intruder aircraft enters the protected area around an aircraft (see Fig. 15.30), TCAS triggers an alarm. The threshold of the area is defined by the time to the Closest Point of Approach (CPA) (the time-to-go is distance divided by closure rate, both combined vertically and horizontally). The protective area can be divided into two regions, one in which a Traffic Advisory (TA) message will be generated and one in which a Resolution Advisory (RA) message will be generated when an intruder appears.

The Traffic Advisory (TA) messages are given to the pilot in form of the word 'TRAFFIC' displayed in yellow on the ND, and the aural voice annunciation, 'traffic, traffic'. This is not the highest alert level. Its purpose is simply to call attention to a potential conflict. TCAS triggers a TA as soon as an intruder enters the TA region. If no altitude data is available from the intruder aircraft, TCAS assumes the intruder's relative altitude is within 1200 feet. If bearing information is available, the intruder can be identified on the ND by a yellow, solid circle. Otherwise, the circle is removed and lateral distance and relative altitude with vertical motion arrow (if motion is detected) is displayed in yellow numbers under the word TRAFFIC'. Resolution Advisory (RA) messages are generated at the highest TCAS alert level and they provide the pilot with aural and visual pitch commands. The pilot must then disengage the autopilot as the escape maneuver has to be flown manually. Any flight director commands (as well as ATC advisories may have to be ignored). The pitch command of an RA always has the highest priority. Note that, if no altitude data is available from the target, an RA will not occur. If bearing information is available, the intruder can be identified on the ND by a red, solid square. If bearing information is not available, the square is removed and lateral distance and relative altitude with vertical motion arrow (if motion is detected) is displayed in red numbers under the word 'TRAFFIC'. Although TCAS is highly regarded, it will have no angular determination warning until TCAS IV/ ACAS III is developed and proved. Several options are available including utilization of GPS systems and Automated En- route Air Traffic (AERA) systems with up to 99.99% accuracy rates. AERA will evaluate all aircraft positions, altitude and speed. The intention is to improve the autonomy of aircraft and thereby significantly reduce ATC involvement.
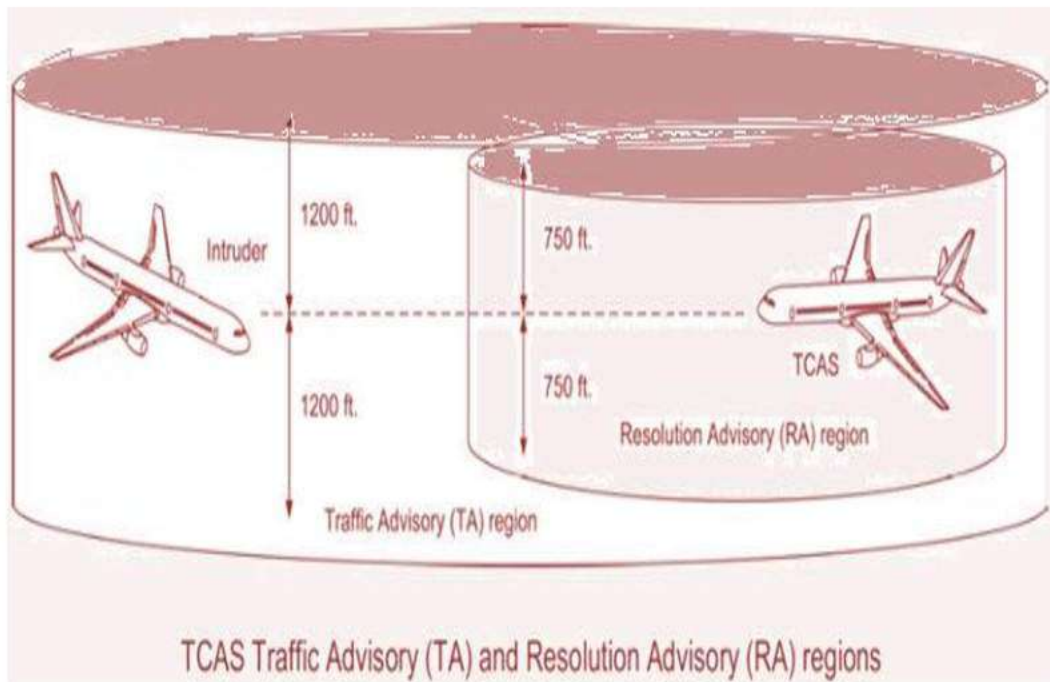
TCAS Traffic Advisory (TA) and Resolution Advisory (RA) regions

Figure15.23